Compal Confidential

ZAMB0/ZAMC0 M/B Schematics Document

AMD Kaveri(FP3) + Bolton(M3)

AMD TOPAZ S3

2014-2-24
REV : 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title: Cover Page
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				Date: Friday, March 07, 2014; Sheet 1 of 50

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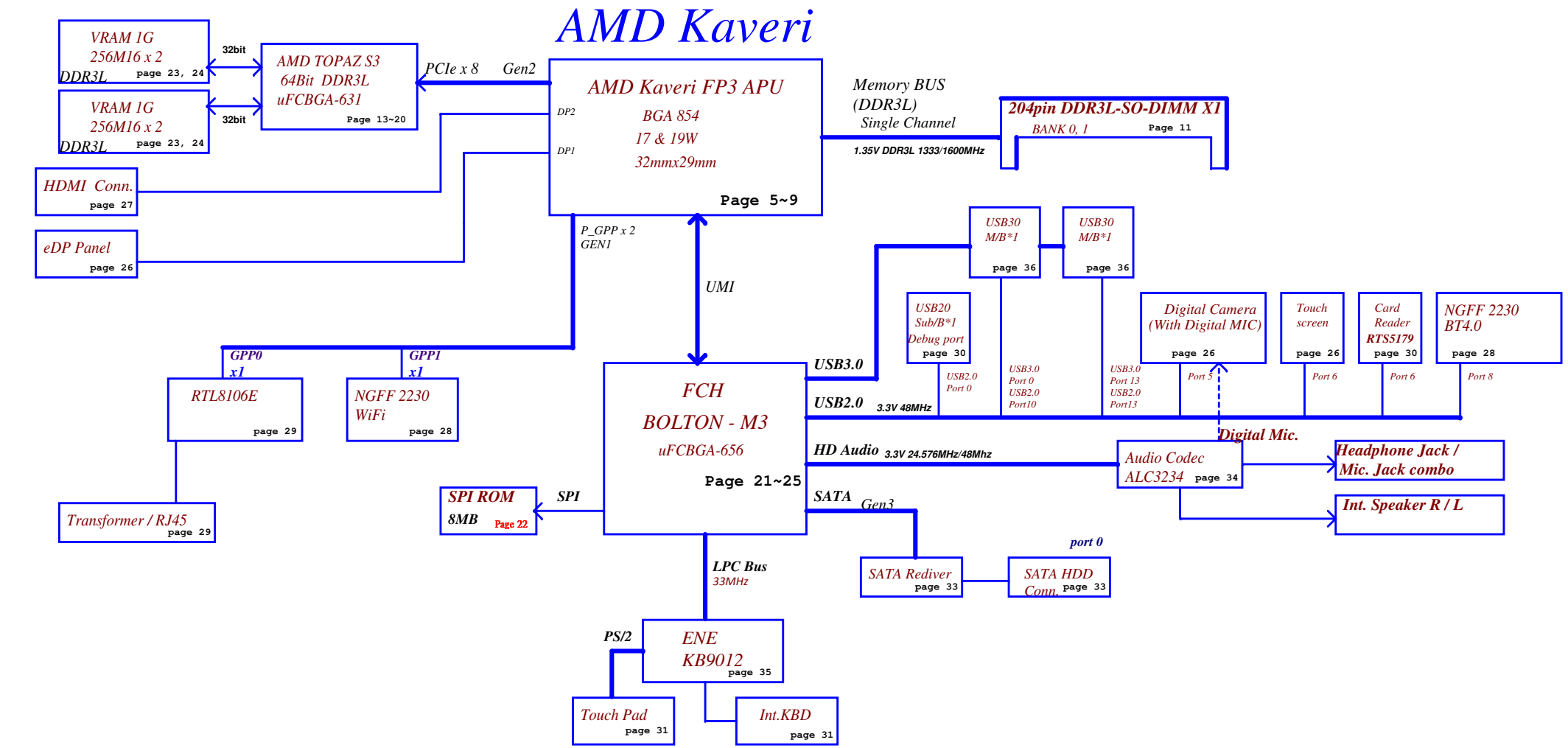
Model Name : ZAMB0/ZAMC0



LED page 30

RTC CKT. page 21 ~ 40

Power On/Off CKT. page 31

Fan Control page 31

DC/DC Interface CKT. page 37

Power Circuit page 40~50

Sub board

LID SW - Power/B page 32

D/B
-USB20 x1
-Card Reader
SD/MMC 2 IN 1
page 30

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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+VDDCI	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+VGA_PCIE	0.95V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05VS switched power rail for APU	ON	OFF	OFF	OFF
+1.35V	1.35V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF	OFF
+3VGS	3.3V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VS	1.8V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3VALW	3.3V power rail for FCH	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN_NGFF	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ZZZ

PCB
Part Number = DA80010O000
<Part Description>

PCB@

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64

BOARD ID Table

Board ID	UMA	DIS(Topaz)
0	SSI	
1		SSI
2	PT	
3		PT
4	ST	
5		ST
6	1.0	
7		1.0

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger IC	0001 001X b	09H

EC SM Bus2 address

Device	Address	HEX
Fintek thermal sensor	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
MINI CARD		

FCH SM Bus 1 address

Device	Address	HEX

BOM Option Table

BOM Config

BOM Structure	Description	UMA 43XX	OPAL 43XX	JET 43XX
9022@	Use EC 9022			
9012@	Use EC 9012	V	V	
UMA@	Display output from APU (UMA only)	V	V	
VGA@	Use VGA (PX or DIS only)		V	
EDP@	Use eDP Panel		V	
AL@	Use Auto load EC code function			
AC@	Support AC Function			
NOAC@	No Support AC Function			
		V	V	
CONN@	Connector (Control by ME)	V	V	
HDT@	Debug Connector			
EMC@	EMC Component			
XEMC@	Reservec for EMC			
X76@	VRAM ID Table (Load By X76J)			
128@	VRAM x 8pcs			
OPAL@	ATI OPAL VGA CONTROLLER			
JET@	ATI JET VGA CONTROLLER			
BL@	ATI JET VGA CONTROLLER			
@	Unpop			
TS@	Touch Screen			
NEMI@	Unpop EMI			
NESD@	Unpop ESD			
AOAC@	AOAC Function			
NAOAC@	Non AOAC Function			

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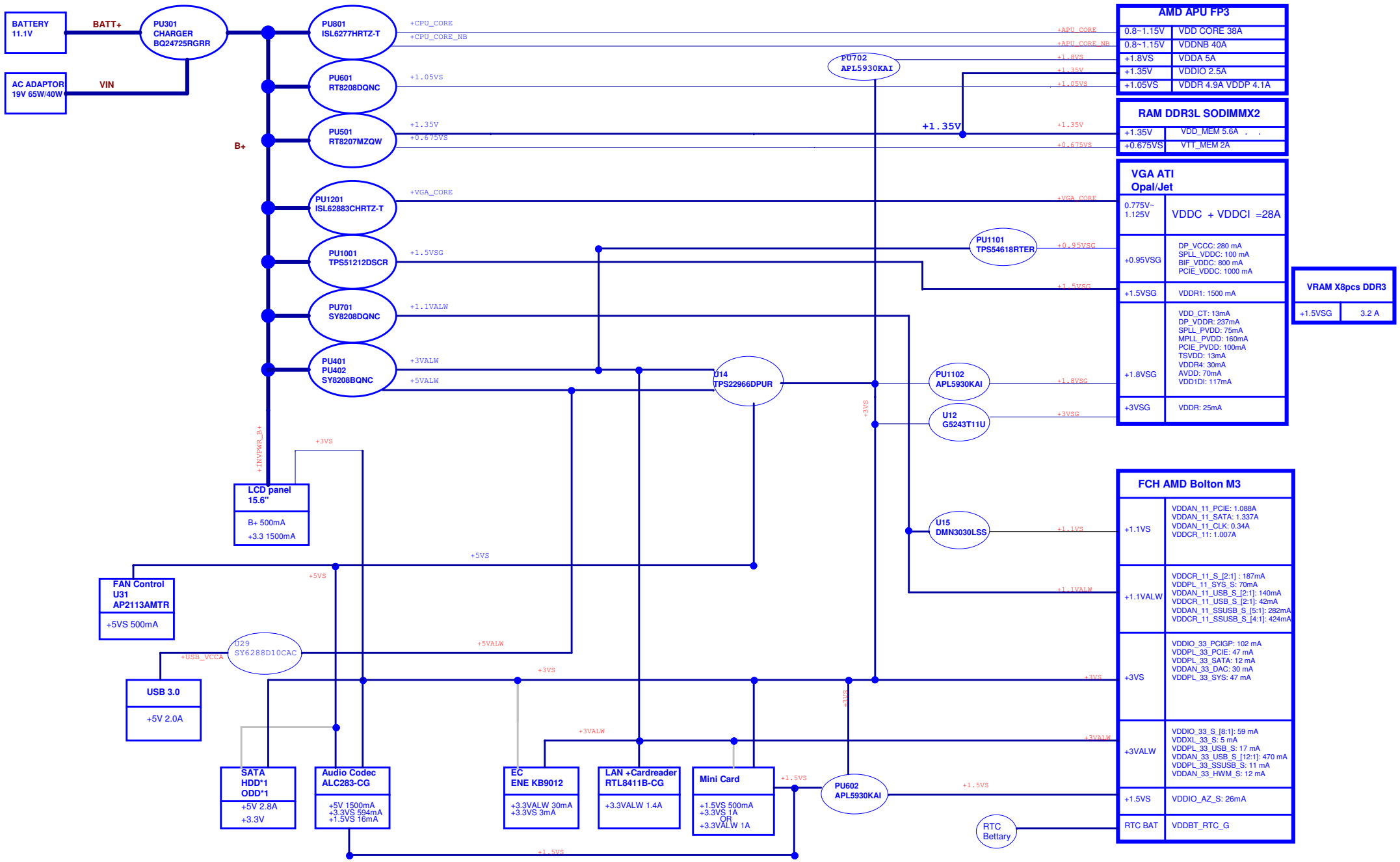

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Title: POWER DELIVERY CHART

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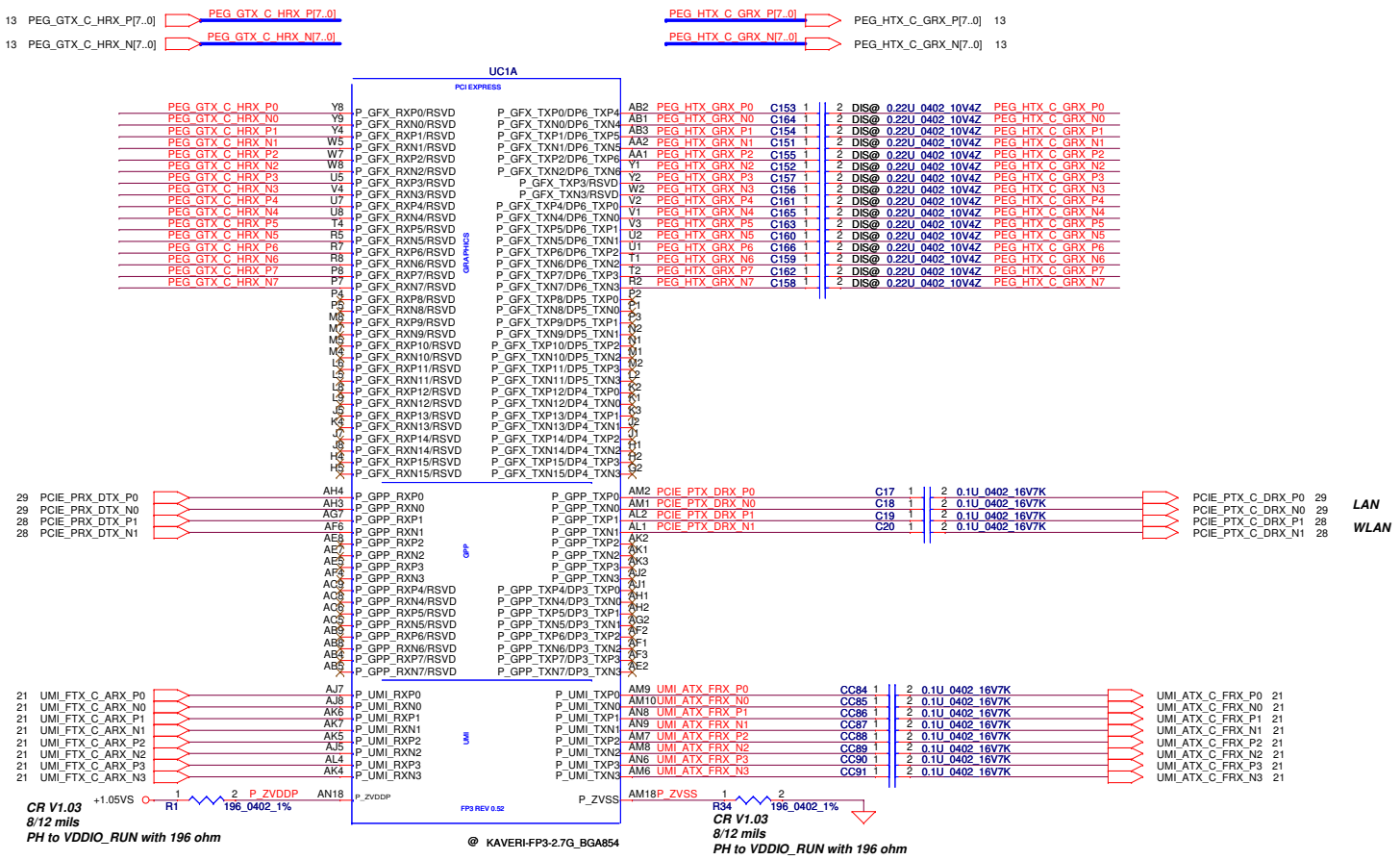

UC1 A8@

UC1 A10@

UC1 FX@

A8-7100 AM7100ECH44JA 1.8G BGA 854P APU A10-7300 AM7300ECH44JA 2G BGA 854P APU FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

SA00007S20L **SA00007S30L** **SA00007TT0L**

AMD, FX-7500, KAVERI, PR	SA00007TT0L	S IC FX-7500 FM7500ECH44JA 2.1G BGA 854P APU
AMD,A10-7300, KAVERI, PR	SA00007S30L	S IC A10-7300 AM7300ECH44JA 2G BGA 854P APU
AMD A8-7100, KAVERI, PR	SA00007S20L	S IC A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

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Title: FP3 PCIE/UMI

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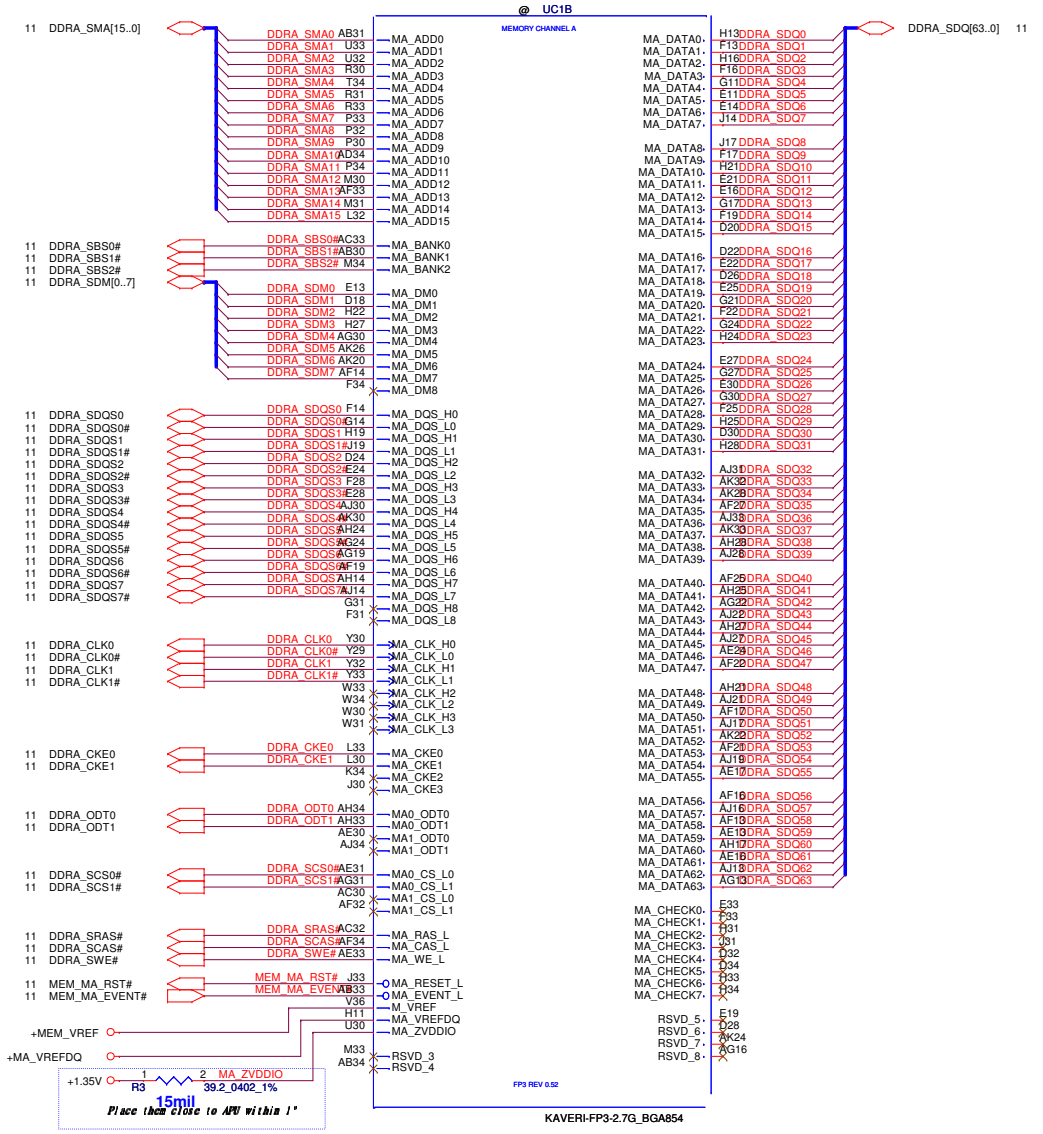
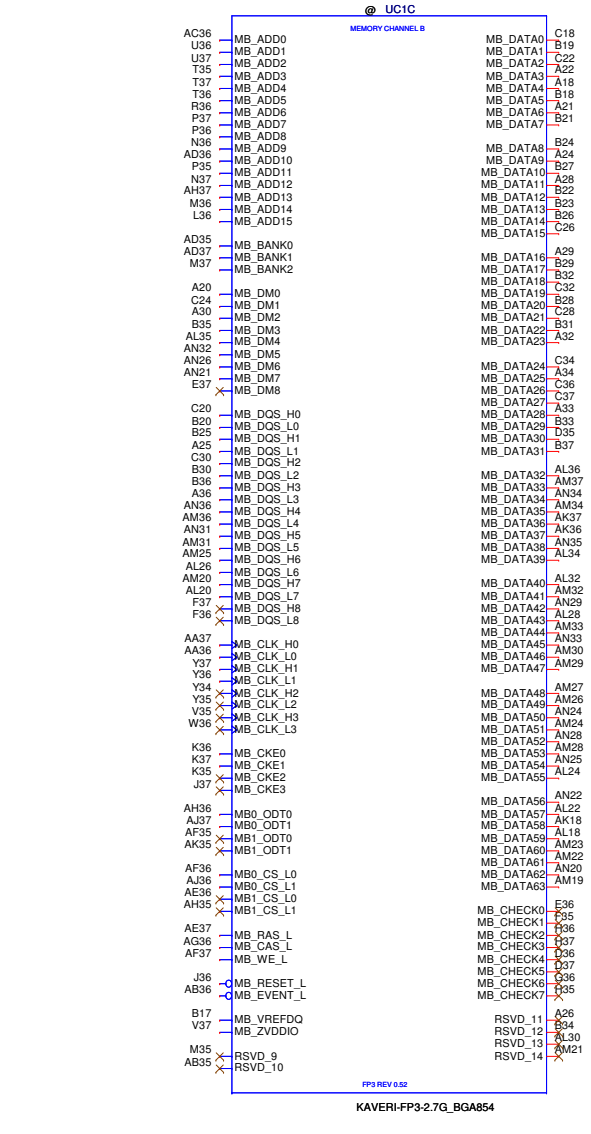
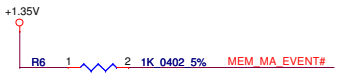


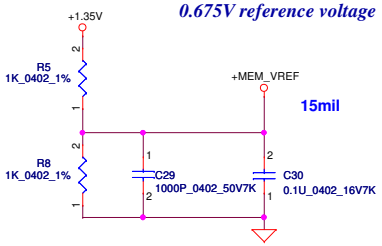


M_VREF (APU)	A	Pull-up resistor to VDDIO	1 kΩ (± 1%)	–	VDDIO
		Pull-down resistor to VSS	1 kΩ (± 1%)	–	VSS
		Decoupling capacitor	0.1 µF	–	VSS
		Decoupling capacitor	1 nF	–	VSS

EVENT# pull high



0.675V reference voltage



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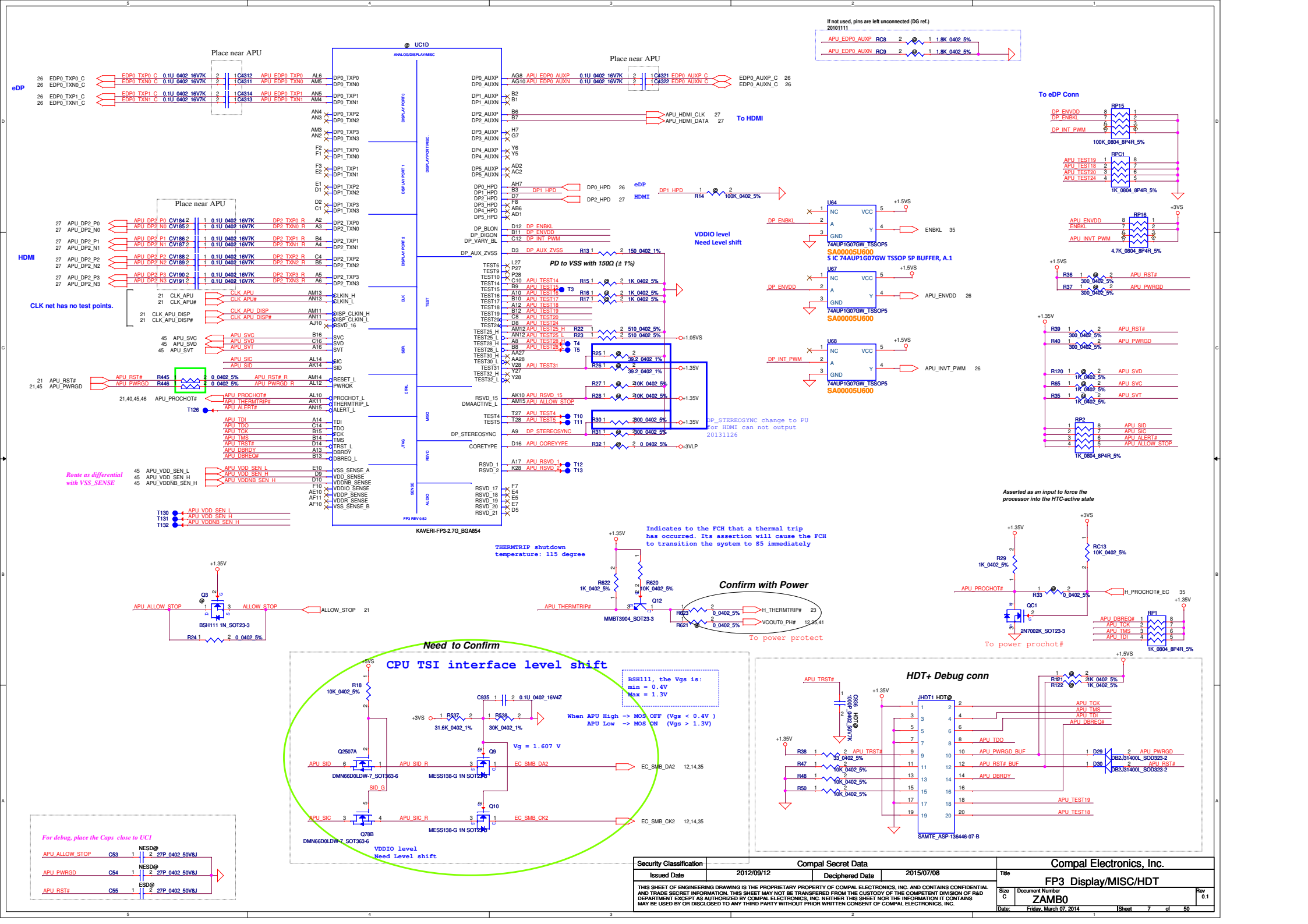

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Title	FP3 Display/MISC/HDT		
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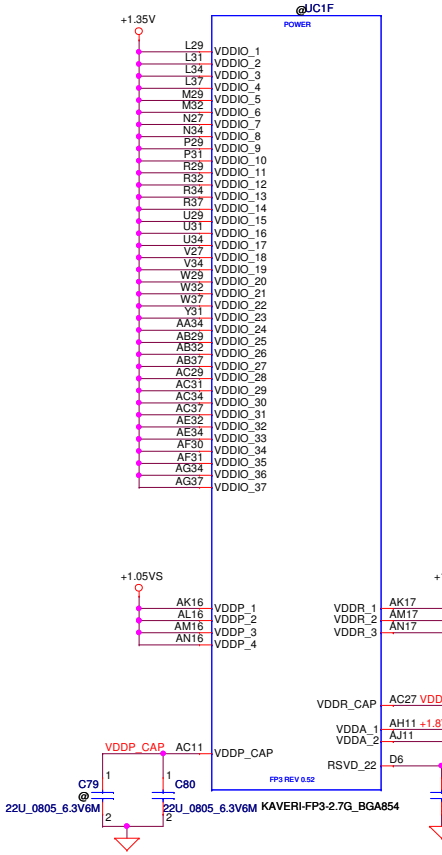
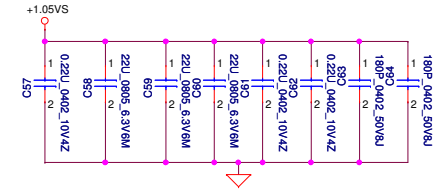
Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.35V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A

+APU_CORE_NB Decoupling Power Side
22uF x10 @ x2
0.22uF x3
180pF x4

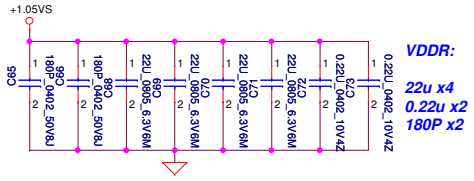
Check list CH47
+APU_CORE Decoupling Power Side
22uF x11 @ x2
0.22uF x2
0.01uF x3
180pF x3



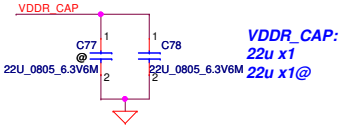
VDDA:
4.7u x1
0.22u x1
3.3n x1



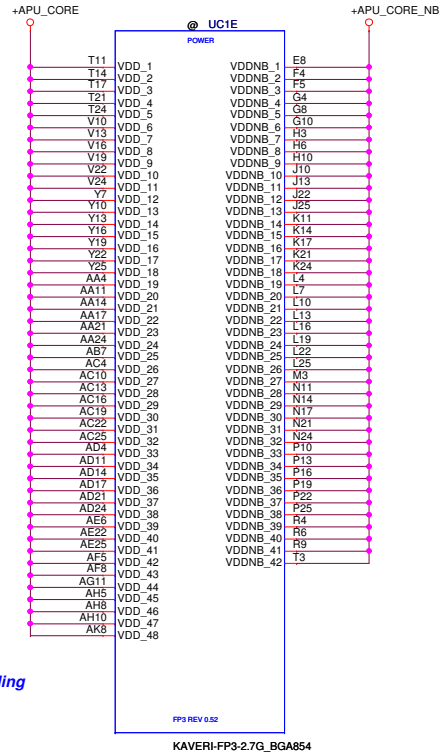
VDDP:
22u x3
0.22u x2
180P x2

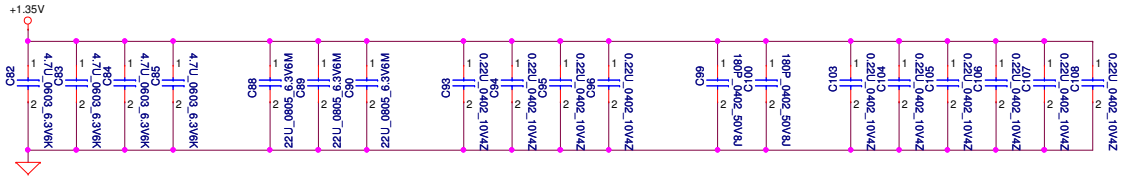


VDDR:
22u x4
0.22u x2
180P x2



VDDR_CAP:
22u x1
22u x1@

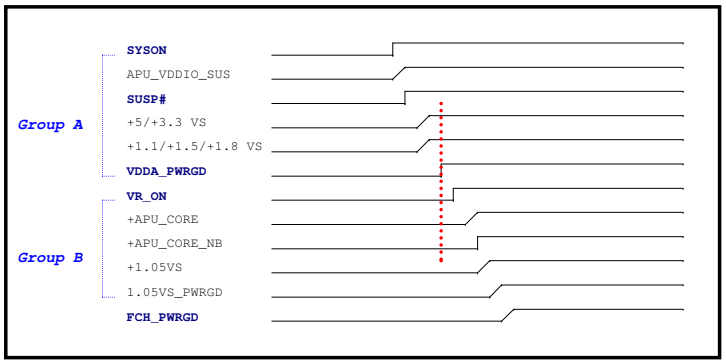




VDDIO Decoupling

22uF x3
4.7uFx4
0.22uF x6
0.22uF x4 (return path)
180pF x2 (return path)

APU sequence : GROUP A need ramp before GROUP B



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Title: FP3 Power

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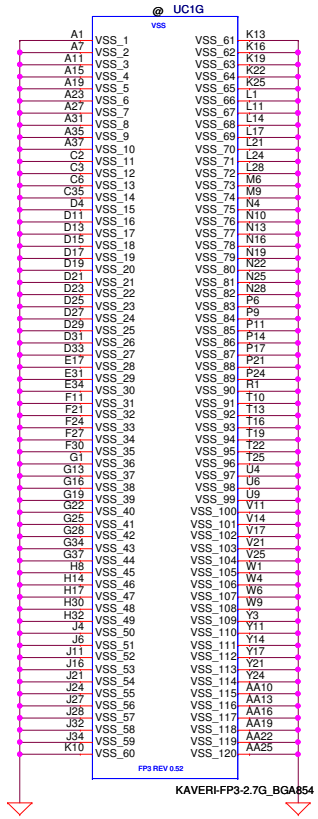

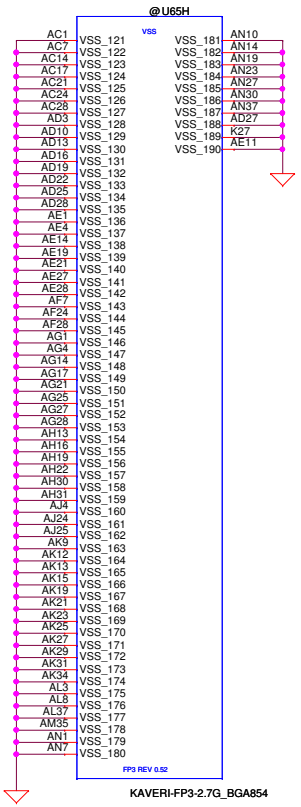

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Title: FP3 GND

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Title: AMD FS1R2 Singal Level Shifter

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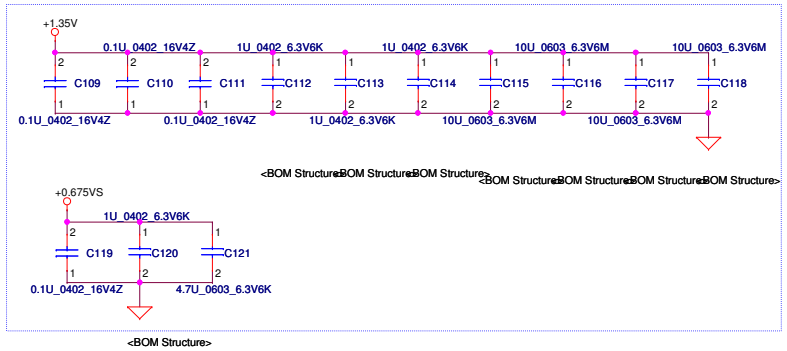
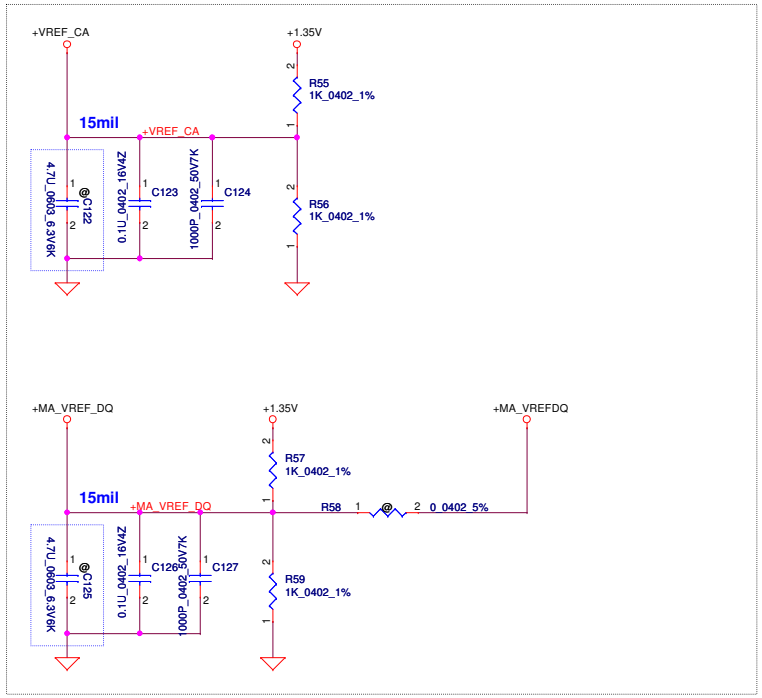
DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 6
DDRA_SDM[0..7] → DDRA_SDM[0..7] 6
DDRA_SMA[0..15] → DDRA_SMA[0..15] 6

Place near DIMM1



Follow CRB design



DIMM_A STD H:4mm

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Title: DIMM_A

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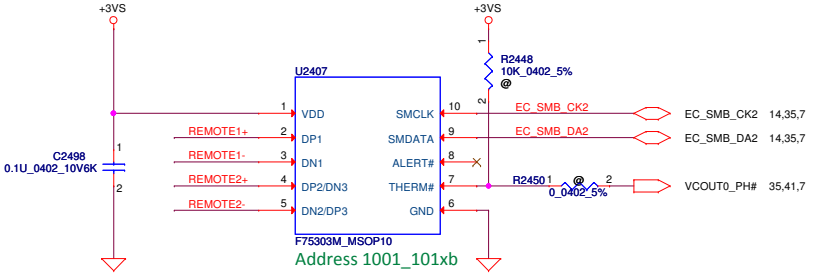
Fintek thermal sensor placed near by DDR3

SA000046C00(S IC EMC1403-2-AIZL-TR MSOP 10P SENSOR)



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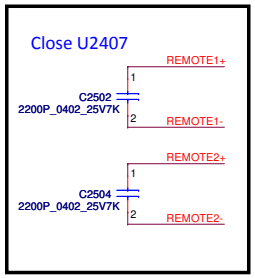
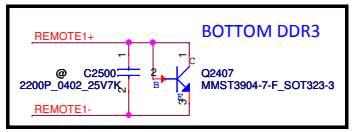
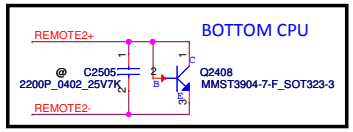
2nd source

SA000029210-->EMC1403-2-AIZL-TR







REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: Thermal Sensor

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 12 of 50

5 PEG_HTX_C_GRX_P[0..7] → PEG_HTX_C_GRX_P[0..7]

5 PEG_HTX_C_GRX_N[0..7] → PEG_HTX_C_GRX_N[0..7]

PEG_GTX_C_HRX_P[0..7] → PEG_GTX_C_HRX_P[0..7] 5

PEG_GTX_C_HRX_N[0..7] → PEG_GTX_C_HRX_N[0..7] 5

UV1 TOPAZ@

TOPAZ XT S3 FCBGA 631P GPU 0FD

SA000079N0L

UV1 JET@

JET XT S3 FCBGA 631P GPU 0FD

SA00007A50L

@ UV1A

PEG_HTX_C_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PEG_GTX_HRX_P0	0.22U_0402_16V7K	2	1	CV1	DIS@	PEG_GTX_C_HRX_P0
PEG_HTX_C_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PEG_GTX_HRX_N0	0.22U_0402_16V7K	2	1	CV2	DIS@	PEG_GTX_C_HRX_N0
PEG_HTX_C_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PEG_GTX_HRX_P1	0.22U_0402_16V7K	2	1	CV3	DIS@	PEG_GTX_C_HRX_P1
PEG_HTX_C_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PEG_GTX_HRX_N1	0.22U_0402_16V7K	2	1	CV4	DIS@	PEG_GTX_C_HRX_N1
PEG_HTX_C_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PEG_GTX_HRX_P2	0.22U_0402_16V7K	2	1	CV5	DIS@	PEG_GTX_C_HRX_P2
PEG_HTX_C_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PEG_GTX_HRX_N2	0.22U_0402_16V7K	2	1	CV6	DIS@	PEG_GTX_C_HRX_N2
PEG_HTX_C_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PEG_GTX_HRX_P3	0.22U_0402_16V7K	2	1	CV7	DIS@	PEG_GTX_C_HRX_P3
PEG_HTX_C_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PEG_GTX_HRX_N3	0.22U_0402_16V7K	2	1	CV8	DIS@	PEG_GTX_C_HRX_N3
PEG_HTX_C_GRX_P4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PEG_GTX_HRX_P4	0.22U_0402_16V7K	2	1	CV13	DIS@	PEG_GTX_C_HRX_P4
PEG_HTX_C_GRX_N4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PEG_GTX_HRX_N4	0.22U_0402_16V7K	2	1	CV16	DIS@	PEG_GTX_C_HRX_N4
PEG_HTX_C_GRX_P5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PEG_GTX_HRX_P5	0.22U_0402_16V7K	2	1	CV35	DIS@	PEG_GTX_C_HRX_P5
PEG_HTX_C_GRX_N5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PEG_GTX_HRX_N5	0.22U_0402_16V7K	2	1	CV30	DIS@	PEG_GTX_C_HRX_N5
PEG_HTX_C_GRX_P6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PEG_GTX_HRX_P6	0.22U_0402_16V7K	2	1	CV12	DIS@	PEG_GTX_C_HRX_P6
PEG_HTX_C_GRX_N6	W31	PCIE_RX6N	PCIE_TX6N	AB26	PEG_GTX_HRX_N6	0.22U_0402_16V7K	2	1	CV14	DIS@	PEG_GTX_C_HRX_N6
PEG_HTX_C_GRX_P7	W29	PCIE_RX7P	PCIE_TX7P	Y27	PEG_GTX_HRX_P7	0.22U_0402_16V7K	2	1	CV31	DIS@	PEG_GTX_C_HRX_P7
PEG_HTX_C_GRX_N7	V28	PCIE_RX7N	PCIE_TX7N	Y26	PEG_GTX_HRX_N7	0.22U_0402_16V7K	2	1	CV32	DIS@	PEG_GTX_C_HRX_N7
	V30	NC#V30	NC#W24	W24							
	U31	NC#U31	NC#W23	W23							
	U29	NC#U29	NC#V27	V27							
	T28	NC#T28	NC#U26	U26							
	T30	NC#T30	NC#U24	U24							
	R31	NC#R31	NC#U23	U23							
	R29	NC#R29	NC#T26	T26							
	P28	NC#P28	NC#T27	T27							
	P30	NC#P30	NC#T24	T24							
	N31	NC#N31	NC#T23	T23							
	N29	NC#N29	NC#P27	P27							
	M28	NC#M28	NC#P26	P26							
	M30	NC#M30	NC#P24	P24							
	L31	NC#L31	NC#P23	P23							
	L29	NC#L29	NC#M27	M27							
	K30	NC#K30	NC#N26	N26							

PCI EXPRESS INTERFACE

21 CLK_PEG_VGA → CLK_PEG_VGA AK30 PCIE_REFCLKP

21 CLK_PEG_VGA# → CLK_PEG_VGA# AK32 PCIE_REFCLKN

CLOCK

RV2 1 DIS@ 2 1K_0402_1% N10 TEST_PG

PLT_RST_VGA# AL27 PERSTB

CALIBRATION

PCIE_CALR_TX Y22 RV1 1 DIS@ 2 1.69K_0402_1%

PCIE_CALR_RX AA22 RV3 1 DIS@ 2 1K_0402_1%

+VGA_PCIE

2160856030-A0_FCBGA631

No Use GPU Display Port outpud

@ UV1F

VARY_BL	AB11	+VGA_CORE	
DIGON	AB12	TOPAZ	
TXCAP_DPA3P	AL15		
TXCAM_DPA3N	AK14		
TX0P_DPA2P	AH16		
TX0M_DPA2N	AJ15		
TX1P_DPA1P	AL17		
TX1M_DPA1N	AK16		
TX2P_DPA0P	AH18		
TX2M_DPA0N	AJ17		
NC_TXOUT_L3P	AL19		
NC_TXOUT_L3N	AK18		
TMDP			
TXCBP_DPB3P	AH20		
TXCBM_DPB3N	AJ19		
TX3P_DPB2P	AL21		
TX3M_DPB2N	AK20		
TX4P_DPB1P	AH22		
TX4M_DPB1N	AJ21		
TX5P_DPB0P	AL23		
TX5M_DPB0N	AK22		
NC_TXOUT_U3P	AK24		
NC_TXOUT_U3N	AJ23		

2160856030-A0_FCBGA631

DGPU_HOLD_RST#(GPIO191)

23 PXS_RST# → PXS_RST#

21 APU_PCIE_RST# → APU_PCIE_RST#

PLT_RST#

+3VGS

UV2 DIS@

PLT_RST_VGA#

RV4 100K_0402_5% DIS@

MC74VHC1G08DFT2G_SC70-5

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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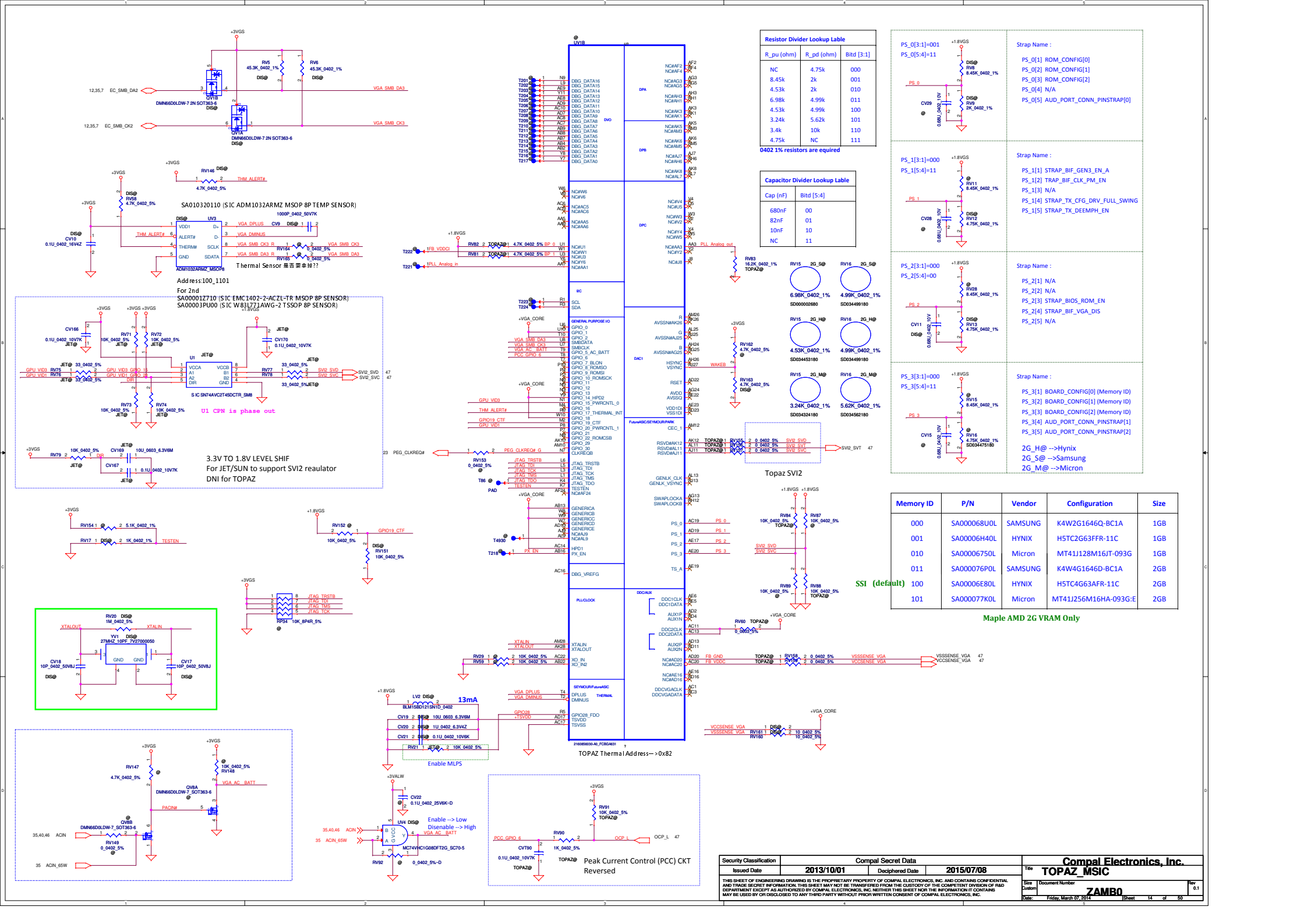
Compal Electronics, Inc.

Title: TOPAZ_PCIE/DP

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 13 of 50



Resistor Divider Lookup Lable		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=00

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

2G_H@ -->Hynix
2G_S@ -->Samsung
2G_M@ -->Micron

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U0L	SAMSUNG	K4W2G1646Q-BC1A	1GB
001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16JT-093G	1GB
011	SA000076P0L	SAMSUNG	K4W4G1646D-BC1A	2GB
SSI (default) 100	SA00006E80L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G:E	2GB

Maple AMD 2G VRAM Only

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

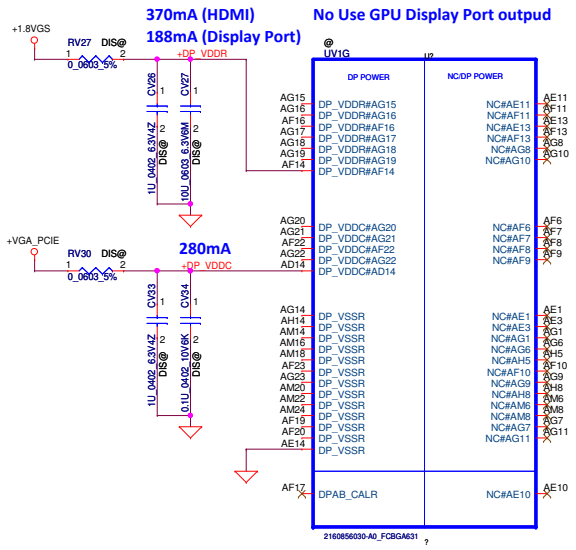
Title: TOPAZ_MSIC

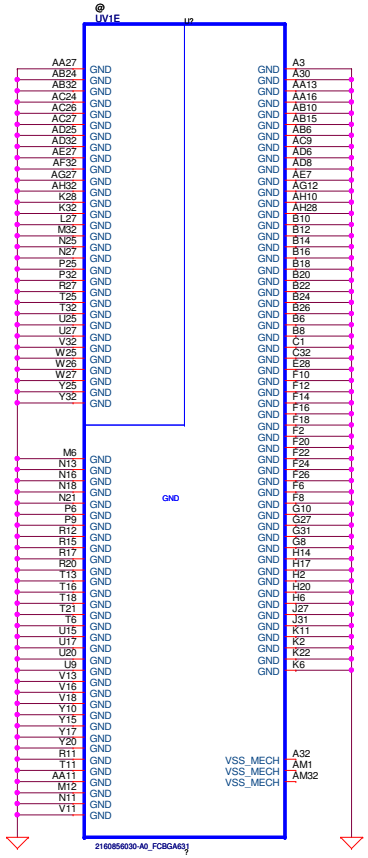
Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 14 of 50

+1.35VS_VGA TO +1.35V_MEM_GFX

JP9 DEFAULT SHORT





Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: **TOPAZ_Power/GND**

Size: Custom | Document Number: **ZAMB0** | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 15 of 50

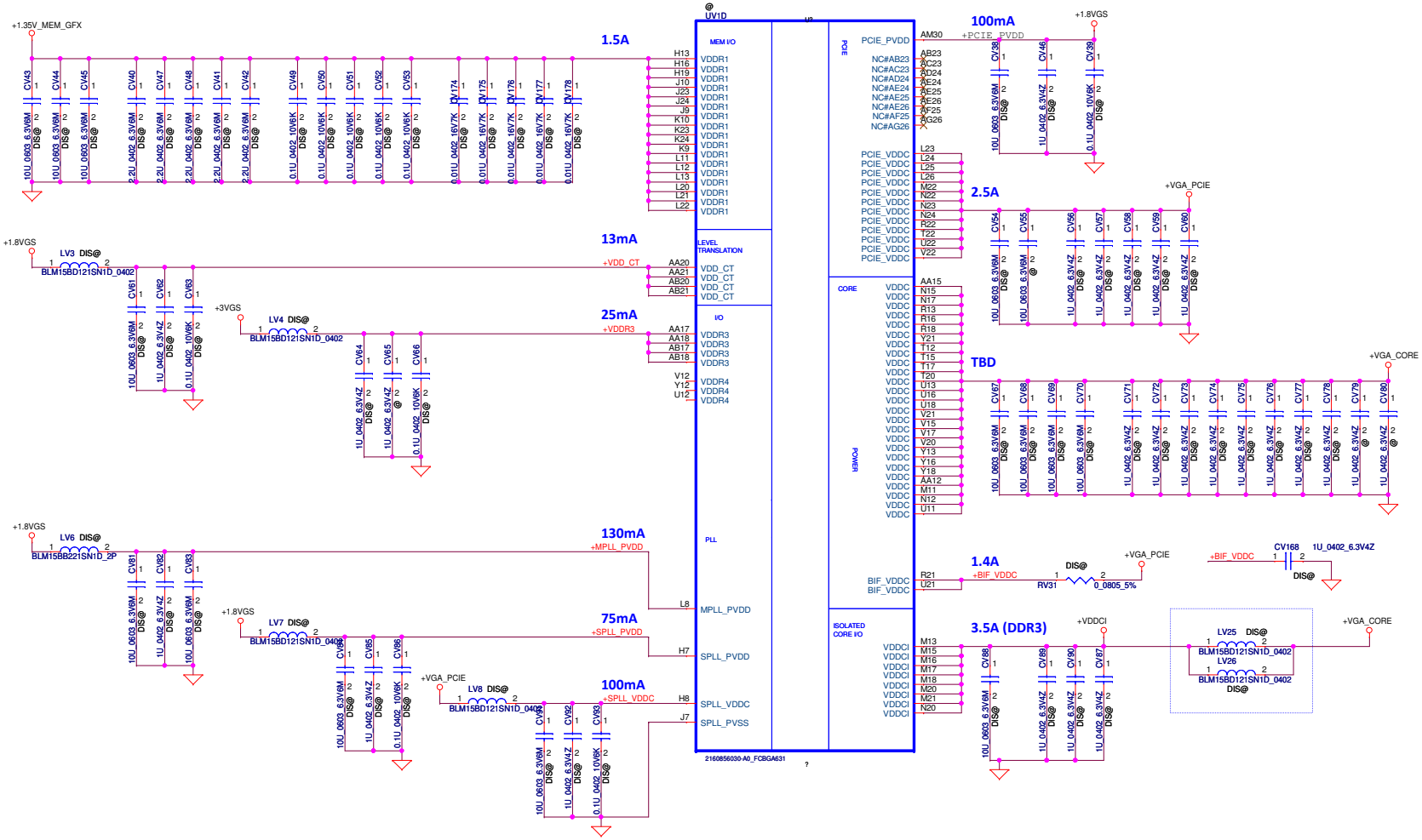
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+VGA_PCIE		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	1	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX		10uF	2.2uF	0.1uF	0.01uF
VDDR1	1.5A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: TOPAZ_Power

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 16 of 50

18,19 M_DA[63..0] M_DA[63..0]
18,19 M_MA[15..0] M_MA[15..0]
18,19 M_DQM[7..0] M_DQM[7..0]
18,19 M_DQS[7..0] M_DQS[7..0]
18,19 M_DQS#[7..0] M_DQS#[7..0]

+1.35V_MEM_GFX
DIS@ RV33 40.2_0402_1% +MVREFDA
DIS@ RV34 100_0402_1%
DIS@ CV94 1U_0402_6.3V4Z

+1.35V_MEM_GFX
DIS@ RV32 40.2_0402_1% +MVREFSA
DIS@ RV35 100_0402_1%
DIS@ CV95 1U_0402_6.3V4Z

18,19 DRAM_RST#
DIS@ RV36 49.9_0402_1%
DIS@ RV37 10_0402_1%
DRAM_RST
DIS@ CV96 120P_0402_50V8J
DIS@ RV38 5.1K_0402_1%
@ CV97 68P_0402_50V8J

Place close to GPU (within 25mm)
and place componment close to each other

@ UV1C U2
GDDR5/DDR3

M_DA0	K27	DQA0_0	MAA0_0/MAA_0	K17	M_MA0
M_DA1	J29	DQA0_1	MAA0_1/MAA_1	J20	M_MA1
M_DA2	H30	DQA0_2	MAA0_2/MAA_2	H23	M_MA2
M_DA3	H32	DQA0_3	MAA0_3/MAA_3	G23	M_MA3
M_DA4	G29	DQA0_4	MAA0_4/MAA_4	G24	M_MA4
M_DA5	F28	DQA0_5	MAA0_5/MAA_5	H24	M_MA5
M_DA6	F32	DQA0_6	MAA0_6/MAA_6	J19	M_MA6
M_DA7	F30	DQA0_7	MAA0_7/MAA_7	K19	M_MA7
M_DA8	C30	DQA0_8	MAA0_8/MAA_13	G20	M_MA13
M_DA9	F27	DQA0_9	MAA0_9/MAA_15	L17	M_MA15
M_DA10	A28	DQA0_10			
M_DA11	C28	DQA0_11	MAA1_0/MAA_8	J14	M_MA8
M_DA12	E27	DQA0_12	MAA1_1/MAA_9	K14	M_MA9
M_DA13	G26	DQA0_13	MAA1_2/MAA_10	J11	M_MA10
M_DA14	D26	DQA0_14	MAA1_3/MAA_11	J13	M_MA11
M_DA15	F25	DQA0_15	MAA1_4/MAA_12	H11	M_MA12
M_DA16	A25	DQA0_16	MAA1_5/MAA_BA2	G11	M_BA2
M_DA17	C25	DQA0_17	MAA1_6/MAA_BA0	J16	M_BA0
M_DA18	E25	DQA0_18	MAA1_7/MAA_BA1	L15	M_BA1
M_DA19	D24	DQA0_19	MAA1_8/MAA_14	G14	M_MA14
M_DA20	E23	DQA0_20	MAA1_9/RSVD	L16	
M_DA21	F23	DQA0_21			
M_DA22	D22	DQA0_22	WCKA0_0/DQMA0_0	E32	M_DQM0
M_DA23	F21	DQA0_23	WCKA0B_0/DQMA0_1	E30	M_DQM1
M_DA24	E21	DQA0_24	WCKA0_1/DQMA0_2	A21	M_DQM2
M_DA25	D20	DQA0_25	WCKA0B_1/DQMA0_3	C21	M_DQM3
M_DA26	F19	DQA0_26	WCKA1_0/DQMA1_0	E13	M_DQM4
M_DA27	A19	DQA0_27	WCKA1B_0/DQMA1_1	D12	M_DQM5
M_DA28	D18	DQA0_28	WCKA1_1/DQMA1_2	E3	M_DQM6
M_DA29	F17	DQA0_29	WCKA1B_1/DQMA1_3	F4	M_DQM7
M_DA30	A17	DQA0_30			
M_DA31	C17	DQA0_31	EDCA0_0/QSA0_0	H28	M_DQS0
M_DA32	E17	DQA1_0	EDCA0_1/QSA0_1	C27	M_DQS1
M_DA33	D16	DQA1_1	EDCA0_2/QSA0_2	A23	M_DQS2
M_DA34	F15	DQA1_2	EDCA0_3/QSA0_3	E19	M_DQS3
M_DA35	A15	DQA1_3	EDCA1_0/QSA1_0	E15	M_DQS4
M_DA36	D14	DQA1_4	EDCA1_1/QSA1_1	D10	M_DQS5
M_DA37	F13	DQA1_5	EDCA1_2/QSA1_2	D6	M_DQS6
M_DA38	A13	DQA1_6	EDCA1_3/QSA1_3	G5	M_DQS7
M_DA39	C13	DQA1_7			
M_DA40	E11	DQA1_8	DDBIA0_0/QSA0_0B	H27	M_DQS#0
M_DA41	A11	DQA1_9	DDBIA0_1/QSA0_1B	A27	M_DQS#1
M_DA42	C11	DQA1_10	DDBIA0_2/QSA0_2B	C23	M_DQS#2
M_DA43	F11	DQA1_11	DDBIA0_3/QSA0_3B	C19	M_DQS#3
M_DA44	A9	DQA1_12	DDBIA1_0/QSA1_0B	C15	M_DQS#4
M_DA45	C9	DQA1_13	DDBIA1_1/QSA1_1B	E9	M_DQS#5
M_DA46	F9	DQA1_14	DDBIA1_2/QSA1_2B	C5	M_DQS#6
M_DA47	D8	DQA1_15	DDBIA1_3/QSA1_3B	H4	M_DQS#7
M_DA48	E7	DQA1_16			
M_DA49	A7	DQA1_17	ADBIA0/ODTA0	L18	VRAM_ODT0
M_DA50	C7	DQA1_18	ADBIA1/ODTA1	K16	VRAM_ODT1
M_DA51	F7	DQA1_19			
M_DA52	A5	DQA1_20	CLKA0	H26	M_CLK0
M_DA53	E5	DQA1_21	CLKA0B	H25	M_CLK#0
M_DA54	C3	DQA1_22			
M_DA55	E1	DQA1_23	CLKA1	G9	M_CLK1
M_DA56	G7	DQA1_24	CLKA1B	H9	M_CLK#1
M_DA57	G6	DQA1_25			
M_DA58	G1	DQA1_26	RASA0B	G22	M_RAS#0
M_DA59	G3	DQA1_27	RASA1B	G17	M_RAS#1
M_DA60	J6	DQA1_28			
M_DA61	J1	DQA1_29	CASA0B	G19	M_CAS#0
M_DA62	J3	DQA1_30	CASA1B	G16	M_CAS#1
M_DA63	J5	DQA1_31			
			CSA0B_0	H22	M_CS#0
+MVREFDA	K26	MVREFDA	CSA0B_1	J22	
+MVREFSA	J26	MVREFSA			
	J25		CSA1B_0	G13	M_CS#1
	K25	NC#J25	CSA1B_1	K13	
		MEM_CALRP0			
			CKEA0	K20	M_CKE0
			CKEA1	J17	M_CKE1
DRAM_RST	L10	DRAM_RST			
			WEA0B	G25	M_WE#0
		CLKTESTA	WEA1B	H10	M_WE#1
	K8	CLKTESTB			
	L7				

MEMORY INTERFACE

M_BA2 18,19
M_BA0 18,19
M_BA1 18,19
VRAM_ODT0 18
VRAM_ODT1 19
M_CLK0 18
M_CLK#0 18
M_CLK1 19
M_CLK#1 19
M_RAS#0 18
M_RAS#1 19
M_CAS#0 18
M_CAS#1 19
M_CS#0 18
M_CS#1 19
M_CKE0 18
M_CKE1 19
M_WE#0 18
M_WE#1 19

2160856030-A0_FCBGA63

RV39 1 DIS@ 2 120_0402_1%

RV40 @ 1 2 51.1_0402_1% CV98 @1 2 0.1U_0402_16V4Z
RV41 @ 1 2 51.1_0402_1% CV99 @1 2 0.1U_0402_16V4Z

Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation,if not need, DNI.

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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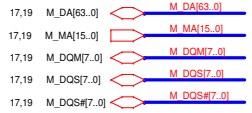
Compal Electronics, Inc.

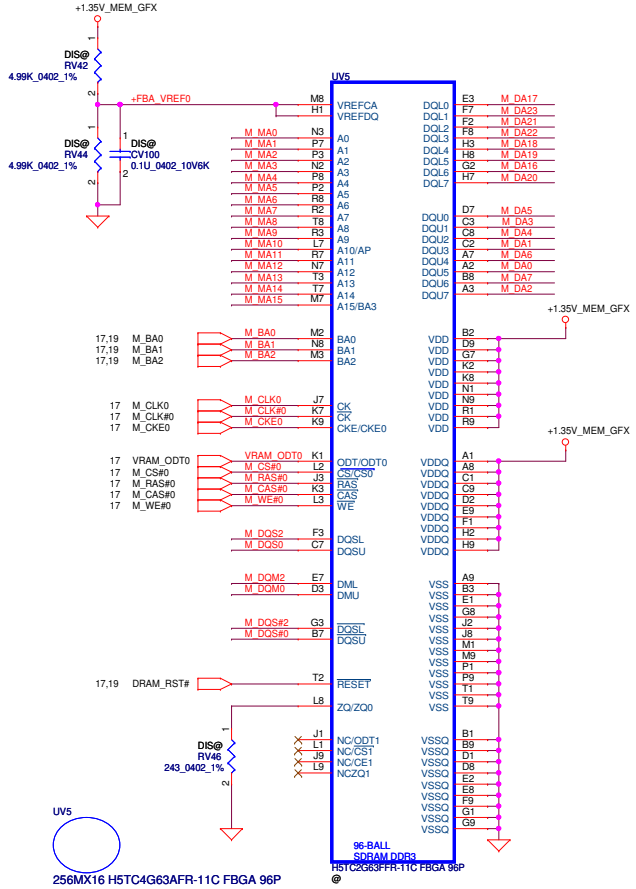
Title: TOPAZ_MEM

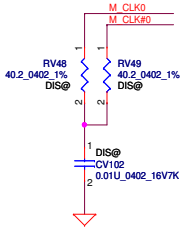
Size: Custom | Document Number: ZAMB0 | Rev: 0.1

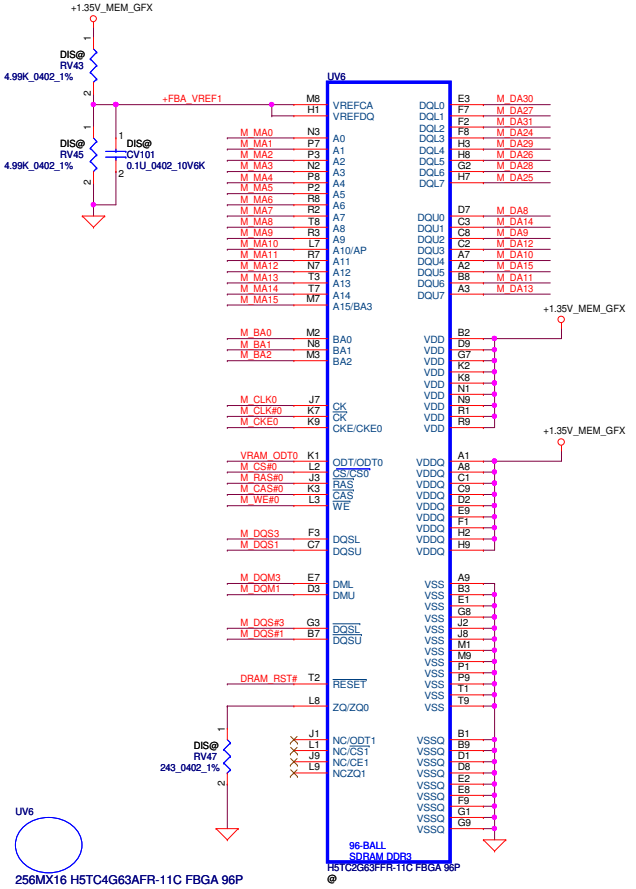
Date: Friday, March 07, 2014 | Sheet 17 of 50

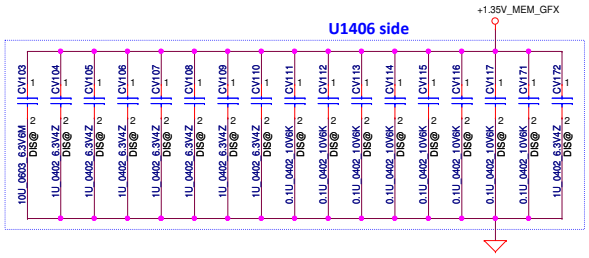
Memory Partition A - Lower 32 bits

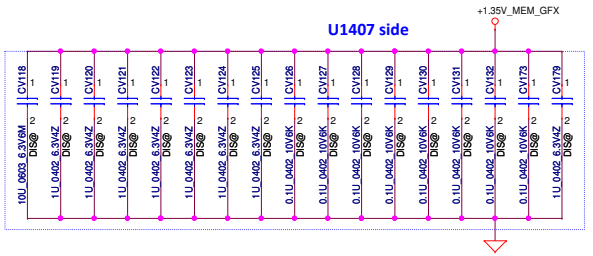












X7655131L04, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design)	
SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design)	
SD034453180, S RES 1/16W 4.53K +-1% 0402, A.1 (Design)	
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)	
X7655131L05, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design)	
SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design)	
SD000002680, S RES 1/16W 6.98K +-1% 0402, A.1 (Design)	
SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)	
X7655131L06, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design)	
SA000077K0L, S IC D3 256M16 MT41J256M16HA-093G:E FBGA, A.4 (Design)	
SD034324180, S RES 1/16W 3.24K +-1% 0402, A.1 (Design)	
SD034562180, S RES 1/16W 5.62K +-1% 0402, A.1 (Design)	

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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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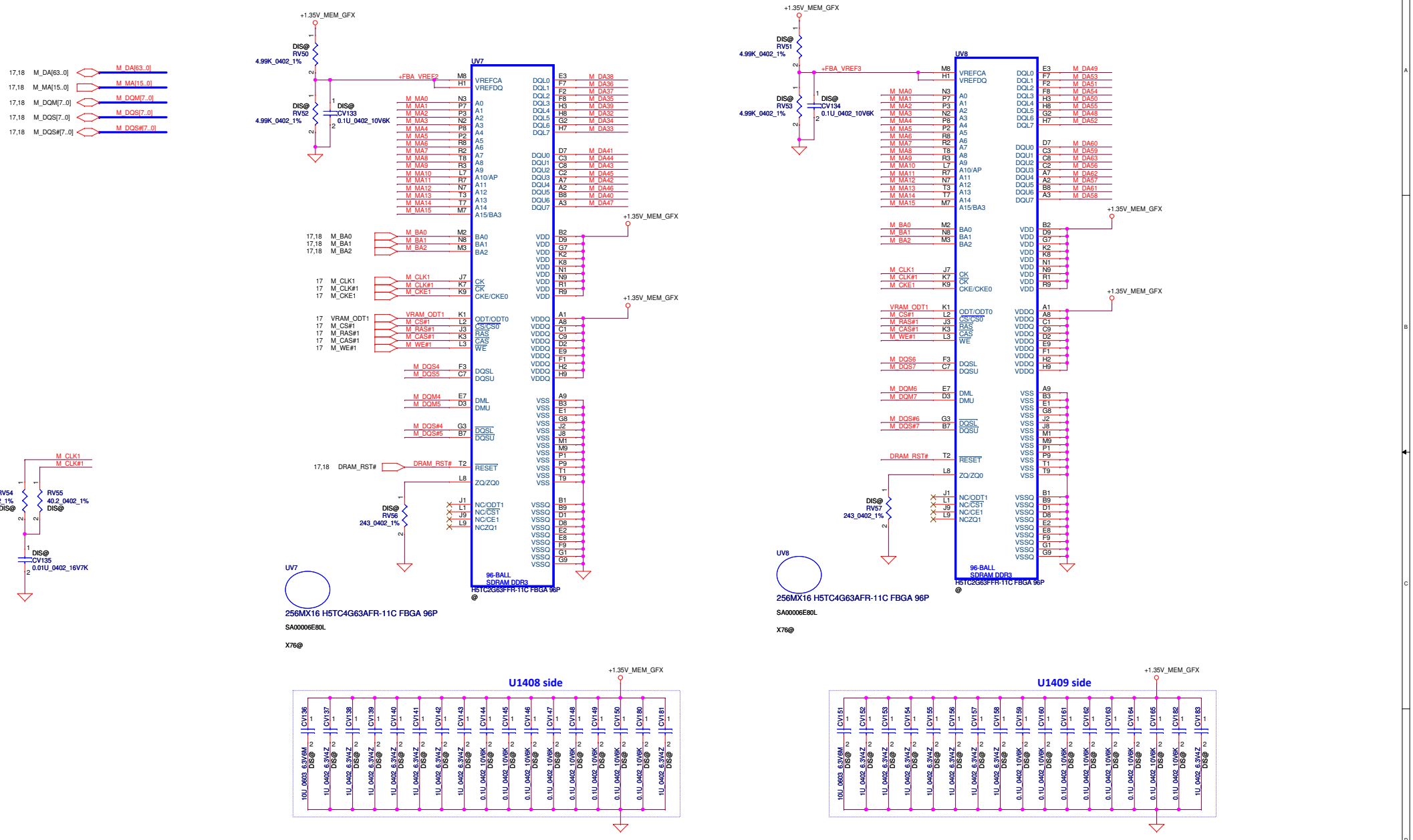
Compal Electronics, Inc.

Title: TOPAZ_VRAM A Lower

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 18 of 50

Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: TOPAZ_VRAM A Upper

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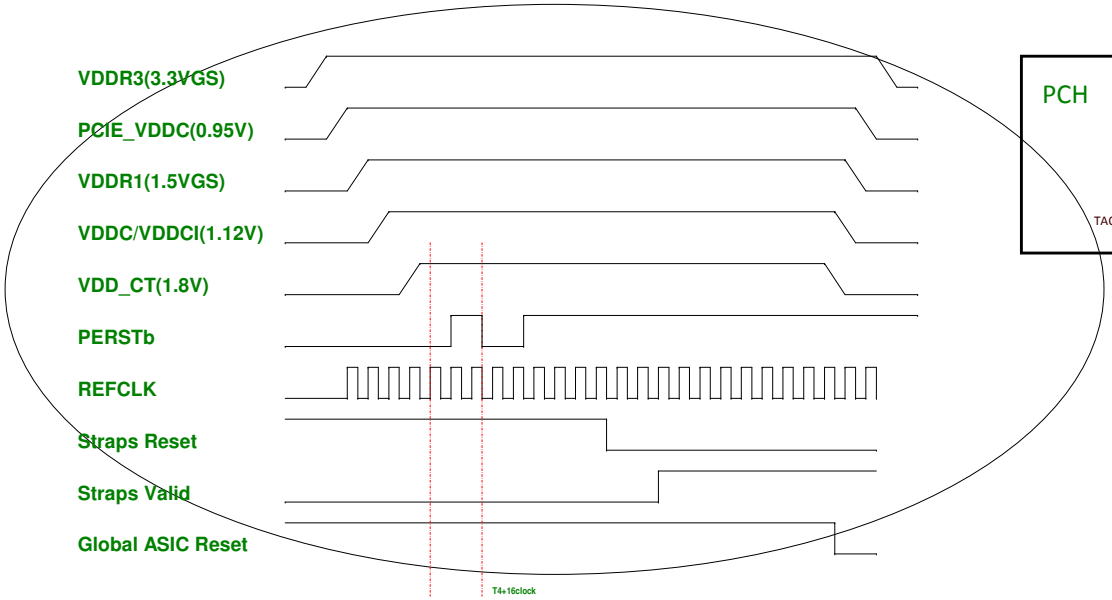
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

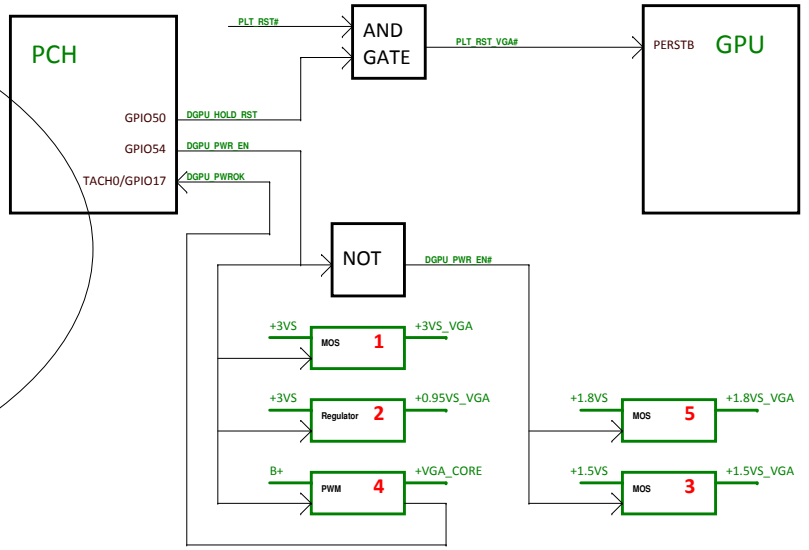
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



CPU part



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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.		
Title: TOPAZ_NOTE		
Size	Document Number: ZAMB0	Rev: 0.1
Date: Friday, March 07, 2014	Sheet 20 of 50	

R90/ C146 close to FCH

RH1 100K_0402_5%
CH6 150P_0402_50V8J
PLT_RST#
RH3 33_0402_5% A_RST#
APU_PCIE_RST#_C

U2A

UMI_FTX_C_ARX_P0 CH7 0.1U_0402_16V7K UMI_FTX_ARX_P0
UMI_FTX_C_ARX_N0 CH1 0.1U_0402_16V7K UMI_FTX_ARX_N0
UMI_FTX_C_ARX_P1 CH8 0.1U_0402_16V7K UMI_FTX_ARX_P1
UMI_FTX_C_ARX_N1 CH2 0.1U_0402_16V7K UMI_FTX_ARX_N1
UMI_FTX_C_ARX_P2 CH9 0.1U_0402_16V7K UMI_FTX_ARX_P2
UMI_FTX_C_ARX_N2 CH3 0.1U_0402_16V7K UMI_FTX_ARX_N2
UMI_FTX_C_ARX_P3 CH4 0.1U_0402_16V7K UMI_FTX_ARX_P3
UMI_FTX_C_ARX_N3 CH5 0.1U_0402_16V7K UMI_FTX_ARX_N3

UMI_ATX_C_FRX_P0
UMI_ATX_C_FRX_N0
UMI_ATX_C_FRX_P1
UMI_ATX_C_FRX_N1
UMI_ATX_C_FRX_P2
UMI_ATX_C_FRX_N2
UMI_ATX_C_FRX_P3
UMI_ATX_C_FRX_N3

+VDDAN_11_PCIE
RH5 590_0402_1% PCIE_CALRP
RH2 2K_0402_1% PCIE_CALRN

Move PCIE device to APU. 20110819

+1.1VS_CKVDD
RH7 2K_0402_1% CLK_CALRN

SS
APU DISP
NSS
APU
dGPU
SS
WLAN
LAN

For "EXT" CLK mode, input to PCIE,

CLK_APU_DISP
CLK_APU_DISP#
CLK_APU
CLK_APU#
CLK_PEG_VGA
CLK_PEG_VGA#
RH10 @ShortPad 0_0402_5% CLK_PCIE_VGA_R
RH11 @ShortPad 0_0402_5% CLK_PCIE_VGA#_R
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
RH12 @ShortPad 0_0402_5% CLK_PCIE_MINI1_R
RH13 @ShortPad 0_0402_5% CLK_PCIE_MINI1#_R
CLK_PCIE_LAN
CLK_PCIE_LAN#
RH15 @ShortPad 0_0402_5% CLK_PCIE_LAN_R
RH16 @ShortPad 0_0402_5% CLK_PCIE_LAN#_R

CLOSE TO RH20
39 LAN_X1
RH17 0_0402_5% CLK_LAN_25M

29 CLK_LAN_25M
CLK_LAN_25M RH20 @ 22_0402_5% CLK_LAN_25M_R

39 PCH_X1
RH21 0_0402_5% 25M_X1
CLOSE TO X1

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU

+3VALW
CH14 @ 0.1U_0402_16V7K
MC74VHC1G08DFT2G SC70 5P
UH1
APU_PCIE_RST# C
@RH25 33_0402_5%
CH16 @ 150P_0402_50V8J
RH26 @ 8.2K_0402_5%
@RH28 0_0402_5%
RH27 0_0402_5% Pad
APU_PCIE_RST# 13
PLT_RST# 28,29,35

R692/ C790 close to FCH

CH12 10P_0402_50V8J
X1 25MHZ_10PF_7V25000014 NGCLK@
CH15 10P_0402_50V8J NGCLK@
RH23 1M_0402_5% NGCLK@
25M_X1
25M_X2

PCIE_RST#
A_RST#
UMI_TX0P
UMI_TX0N
UMI_TX1P
UMI_TX1N
UMI_TX2P
UMI_TX2N
UMI_TX3P
UMI_TX3N
UMI_RX0P
UMI_RX0N
UMI_RX1P
UMI_RX1N
UMI_RX2P
UMI_RX2N
UMI_RX3P
UMI_RX3N
PCIE_CALRP
PCIE_CALRN
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
CLK_CALRN
PCIE_RCLKP
PCIE_RCLKN
DISP_CLKP
DISP_CLKN
DISP2_CLKP
DISP2_CLKN
APU_CLKP
APU_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
GPP_CLK7P
GPP_CLK7N
GPP_CLK8P
GPP_CLK8N
14M_25M_48M_OSC

21807-A13-HUDSON-M3_FCBGA656
Hud@

HUDSON-2

PCI_CLKS
PCICLK0
PCICLK1/GPIO36
PCICLK2/GPIO37
PCICLK3/GPIO38
PCICLK4/14M_OSC/GPIO39
PCIRST#
PCI_CLK1 25
PCI_CLK3 25
PCI_CLK4 25

PCI EXPRESS INTERFACES

PCI INTERFACE
AD0/GPIO0
AD1/GPIO1
AD2/GPIO2
AD3/GPIO3
AD4/GPIO4
AD5/GPIO5
AD6/GPIO6
AD7/GPIO7
AD8/GPIO8
AD9/GPIO9
AD10/GPIO10
AD11/GPIO11
AD12/GPIO12
AD13/GPIO13
AD14/GPIO14
AD15/GPIO15
AD16/GPIO16
AD17/GPIO17
AD18/GPIO18
AD19/GPIO19
AD20/GPIO20
AD21/GPIO21
AD22/GPIO22
AD23/GPIO23 PCI_AD23 25
AD24/GPIO24 PCI_AD24 25
AD25/GPIO25 PCI_AD25 25
AD26/GPIO26 PCI_AD26 25
AD27/GPIO27 PCI_AD27 25
AD28/GPIO28
AD29/GPIO29
AD30/GPIO30
AD31/GPIO31
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42
GNT0#
GNT1#/GPO44
GNT2#/SD_LED/GPO45
GNT3#/CLK_REQ7#/GPIO46
CLKRUN#
LOCK#
INTE#/GPIO32
INTF#/GPIO33
INTG#/GPIO34
INTH#/GPIO35
T99
T107
T108

CLOCK GENERATOR

LPC
LPCCLK0 B25 CLK_EC33M 1 RH14 22_0402_5% CLK_PCI_EC 25,35
LPCCLK1 D25 LPC_CLK1
LAD0 C28 LPC_AD0 35
LAD1 A26 LPC_AD1 35
LAD2 A29 LPC_AD2 35
LAD3 A31 LPC_AD3 35
LFRAME# B27 LPC_FRAME# 35
LDRQ0# AE27
LDRQ1#/CLK_REQ6#/GPIO49 AE19
SERIRQ/GPIO48 SERIRQ 35

APU
DMA_ACTIVE# G25
PROCHOT# E28 APU_PROCHOT#_R RH18 1 @ 2 0_0402_5% ALLOW_STOP 7
APU_PG E26 APU_PWRGD APU_PWRGD 45,7 APU_PROCHOT# 40,45,46,7
LDT_STP# G26
APU_RST# F26 APU_RST# APU_RST# 7

S5_PLUS
S5_CORE_EN H7
RTCCLK F1
INTRUDER_ALERT# F3 RTC_CLK 25,35
VDDBT_RTC_G E6 +VDDBT_RTC
32K_X1 G2 32K_X1
32K_X2 G4 32K_X2

CH10 18P_0402_50V8J NGCLK@
RH4 20M_0402_5% NGCLK@
Y2 32.768KHZ_12.5PF_9H03200019 NGCLK@
CH11 18P_0402_50V8J NGCLK@
32K_X1
32K_X2
Close to HUDSON-M2/3

CLOSE TO Y1
39 FCH_RTCX1
RH6 0_0402_5% 32K_X1

U2 BOIR1@
SA000066K1L
218-0844012 A1 BOLTON-M3 FCH 0FD

U2 BOIR3@
SA000066K2L
218-0844012 A1 BOLTON-M3 FCH A31!

CH17 10P_0402_50V8J
LPC_CLK1

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

+RTCBATT
RH19 510_0402_5%
+3VLP
+VCOIN
+VCOIN_RTC
DH1 RB751V-40_SOD-323
DH2 RB751V-40_SOD-323
W=20mils
RH22 510_0402_5%
CH13 1U_0402_6.3V6K
CLRP1 @ SHORT PADS
RH24 10M_0402_5%
for Clear CMOS

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 21 of 50

8MB SPI ROM

Check CS# PU R 1kor10k and pop/nopop
SCL v1.20 : If an SPI ROM is shared between
the FCH and the Embedded Controller
a 10-K pull-up resistor to +3.3V_S5 is installed.

Place near CONN

HDD

FCH:
Gen2<6"

U2B

HUDSON-2

33 SATA_PTX_DRX_P0_C
33 SATA_PTX_DRX_N0_C
33 SATA_PRX_DTX_N0_C
33 SATA_PRX_DTX_P0_C

AK19 SATA_TX0P
AM19 SATA_TX0N
AL20 SATA_RX0N
AN20 SATA_RX0P
AN22 SATA_TX1P
AL22 SATA_TX1N
AH20 SATA_RX1N
AJ20 SATA_RX1P
AJ22 SATA_TX2P
AH22 SATA_TX2N
AM23 SATA_RX2N
AK23 SATA_RX2P
AH24 SATA_TX3P
AJ24 SATA_TX3N
AN24 SATA_RX3N
AL24 SATA_RX3P
AL26 SATA_TX4P
AN26 SATA_TX4N
AJ26 SATA_RX4N
AH26 SATA_RX4P
AN29 SATA_TX5P
AL28 SATA_TX5N
AK27 SATA_RX5N
AM27 SATA_RX5P
AL29 NC6
AN31 NC7
AL31 NC8
AL33 NC9
AH33 NC10
AH31 NC11
AJ33 NC12
AJ31 NC13

SERIAL ATA

1K_0402_1% RH37 SATA_CALRP AF28 SATA_CALRP
+AVDD_SATA 931_0402_1% RH38 SATA_CALRN AF27 SATA_CALRN

30 HDD_LED# AD22 SATA_ACT#/GPIO67
+3VS RH39 10K_0402_5% AF21 SATA_X1

AG21 SATA_X2

SD_CLK/SCLK_2/GPIO73 AL14
SD_CMD/SLOAD_2/GPIO74 AN14
SD_CD/GPIO75 AJ12
SD_WP/GPIO76 AH12
SD_DATA0/SDATI_2/GPIO77 AK13
SD_DATA1/SDATO_2/GPIO78 AM13
SD_DATA2/GPIO79 AH15
SD_DATA3/GPIO80 AJ14

SD_CARD

GBE_COL AC4
GBE_CRS AD3
GBE_MDCK AD9
GBE_MDIO W10
GBE_RXCLK AB8
GBE_RXD3 AH7
GBE_RXD2 AF7
GBE_RXD1 AE7
GBE_RXD0 AD7
GBE_RXCTL/RXDV AG8
GBE_RXERR AD1
GBE_TXCLK AB7
GBE_TXD3 AF9
GBE_TXD2 AG6
GBE_TXD1 AE8
GBE_TXD0 AD8
GBE_TXCTL/TXEN AB9
GBE_PHY_PD AC2
GBE_PHY_RST# AA7
GBE_PHY_INTR W9 GBE_PHY_INTR

GBE_COL / GBE_CRS / GBE_MDIO
GBE_RXERR / Left unconnected.
FCH SCL V1.20 19-35

GBE_LAN

SPI_DI/GPIO164 V6 FCH_SPI_MISO_R
SPI_DO/GPIO163 V5 FCH_SPI_MOSI_R
SPI_CLK/GPIO162 V3 FCH_SPI_CLK
SPI_CS1#/GPIO165 T6 FCH_SPI_CS1#
ROM_RST#/SPI_WP#/GPIO161 V1 FCH_SPI_WP#

SPI_ROM

VGA_RED L30
VGA_GREEN L32
VGA_BLUE M29
VGA_HSYNC/GPO68 M28
VGA_VSYNC/GPO69 N30
VGA_DDC_SDA/GPO70 M33
VGA_DDC_SCL/GPO71 N32
VGA_DAC_RSET K31
AUX_VGA_CH_P V28
AUX_VGA_CH_N V29
AUXCAL U28

VGA_DAC

ML_VGA_L0P T31
ML_VGA_L0N T33
ML_VGA_L1P T29
ML_VGA_L1N T28
ML_VGA_L2P R32
ML_VGA_L2N R30
ML_VGA_L3P P29
ML_VGA_L3N P28
ML_VGA_HPD/GPIO229 C29

VGA_MAINLINK

+3VS RH41 @ 10K_0402_5% AH16 FANOUT0/GPIO52
AM15 FANOUT1/GPIO53
28 BT_ON# BT_ON# AJ16 FANOUT2/GPIO54
AK15 FANIN0/GPIO56
28 WL_OFF# WL_OFF# AN16 FANIN1/GPIO57
RH40 @ 10K_0402_5% AL16 FANIN2/GPIO58
T129 ODD_EN K6 TEMPIN0/GPIO171
GPIO172 K5 TEMPIN1/GPIO172
GPIO173 K3 TEMPIN2/GPIO173
T127 APU_ALERT#_FCH M6 TEMPIN3/TALERT#/GPIO174

HW MONITOR

VIN0/GPIO175 N2 GPIO175
VIN1/GPIO176 M3 GPIO176
VIN2/SDATI_1/GPIO177 L2 GPIO177
VIN3/SDATO_1/GPIO178 N4 GPIO178
VIN4/SLOAD_1/GPIO179 P1 GPIO179
VIN5/SCLK_1/GPIO180 P3 GPIO180
VIN6/GBE_STAT3/GPIO181 M1 GPIO181
VIN7/GBE_LED3/GPIO182 M5 GPIO182

NC1 AG16
NC2 AH16
NC3 A28
NC4 G27
NC5 L4

21807-A13-HUDSON-M3_FCBGA656

Hud@

+3VALW
0.1U_0402_16V4Z CH466

USPI1
FCH_SPI_CS1# 1 CS# VCC 8 FCH_SPI_VCC
FCH_SPI_MISO 2 DO(IO1) HOLD#(IO3) 7 FCH_SPI_HOLD#
FCH_SPI_WP# 3 WP#(IO2) CLK 6 FCH_SPI_CLK
4 GND DI(IO0) 5 FCH_SPI_MOSI
EN25QH64-104HIP_SO8

FCH_SPI_MISO_R 33_0402_5% RH34
FCH_SPI_HOLD# 23
FCH_SPI_MOSI_R 33_0402_5% RH35
FCH_SPI_CLK

RH29 33_0402_5% NEMI@
CH20 22P_0402_50V8J NEMI@

+3VALW
RPH6
FCH_SPI_CS1# GBE_PHY_INTR FCH_SPI_WP# FCH_SPI_HOLD#
10K_0804_8P4R_5%

GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-KΩ 5% resistor.
FCH SCL v1.20 #19-85

Removed RGMII/MII support and updated termination
requirements for GBE_COL, GBE_CRS, GBE_RXERR
and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20

FCH_SPI_CS1# RH65 AL@ 0_0402_5% EC_SPI_CS1# 35
FCH_SPI_MISO RH67 AL@ 0_0402_5% EC_SPI_MISO 35
FCH_SPI_MOSI RH69 AL@ 0_0402_5% EC_SPI_MOSI 35
FCH_SPI_CLK RH70 AL@ 0_0402_5% EC_SPI_CLK 35

+3VALW
23 USB_OC5#
RPH1 USB_OC5# GPIO180 GPIO179 APU_ALERT#_FCH
10K_0804_8P4R_5%
RPH3 GPIO182 GPIO177 GPIO172 GPIO173
10K_0804_8P4R_5%
RPH2 GPIO175 GPIO178 GPIO181 GPIO176
10K_0804_8P4R_5%

Need to enable internal
pull down to leave
unconnected

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Issued Date	2012/09/11	Deciphered Date	2015/07/08

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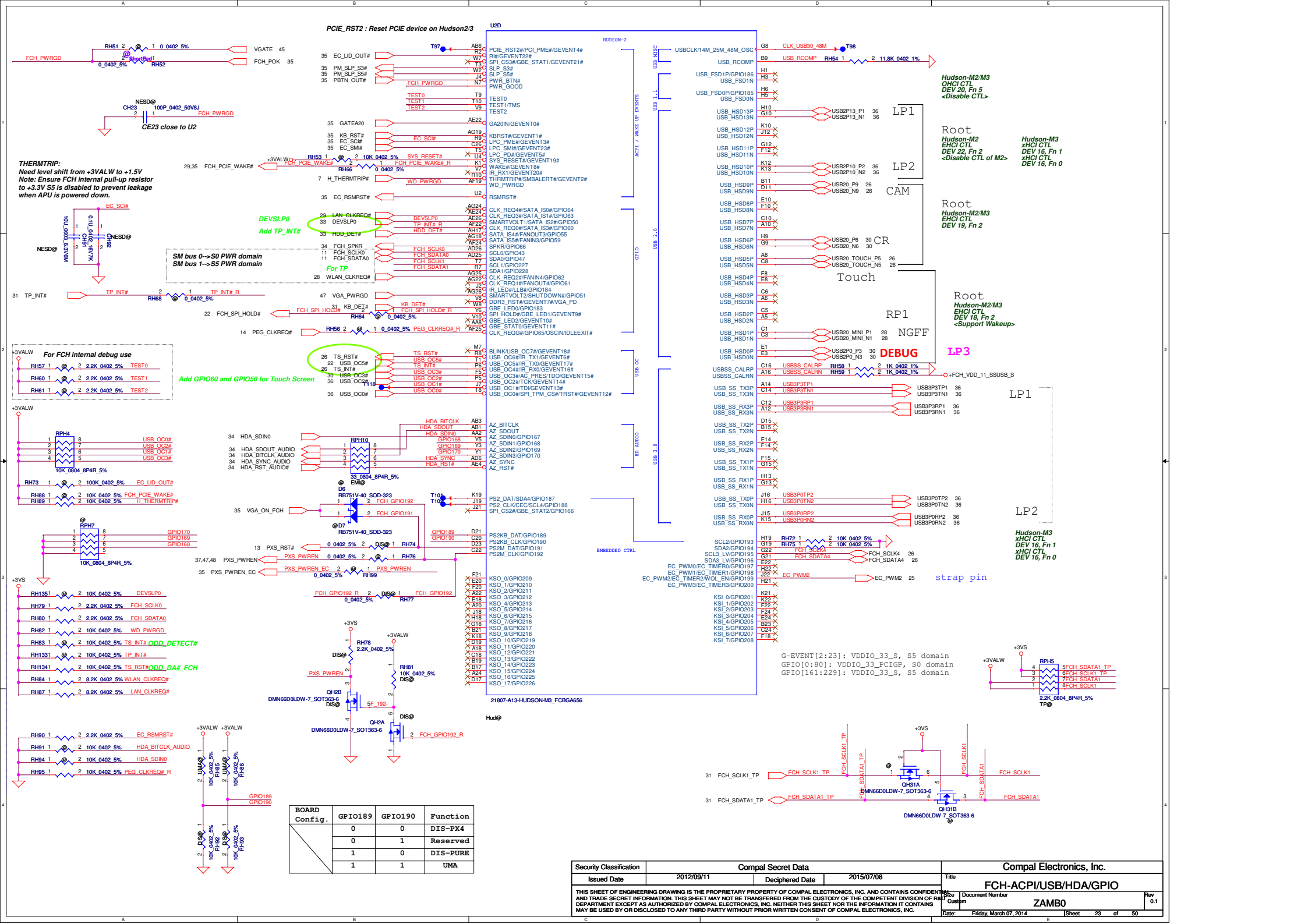
Compal Electronics, Inc.

Title: FCH SATA/SPI/VGA/HWM/SD

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 22 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

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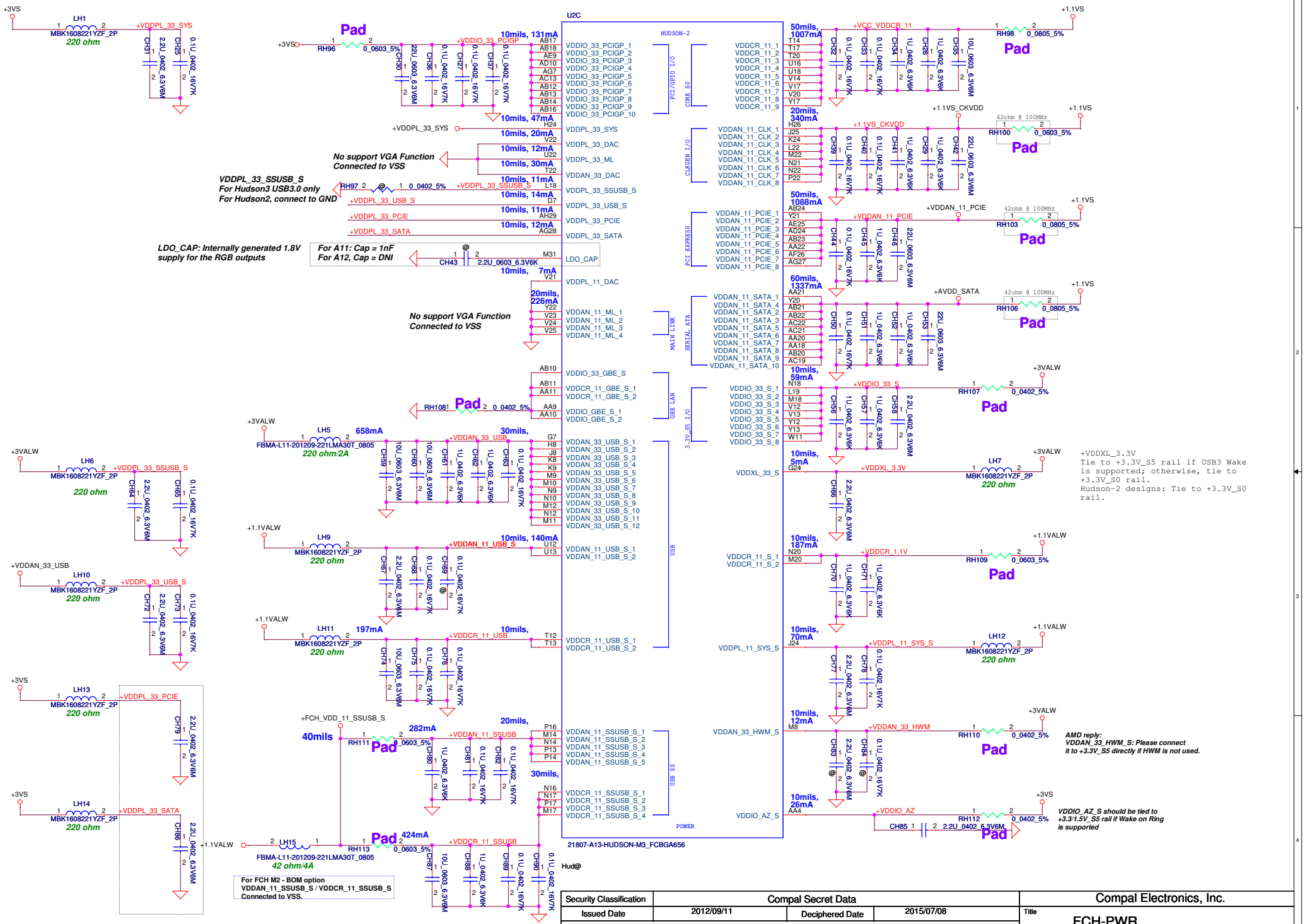
Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size	Document Number	Rev
Custom	ZAMB0	0.1

Date: Friday, March 07, 2014 Sheet 23 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

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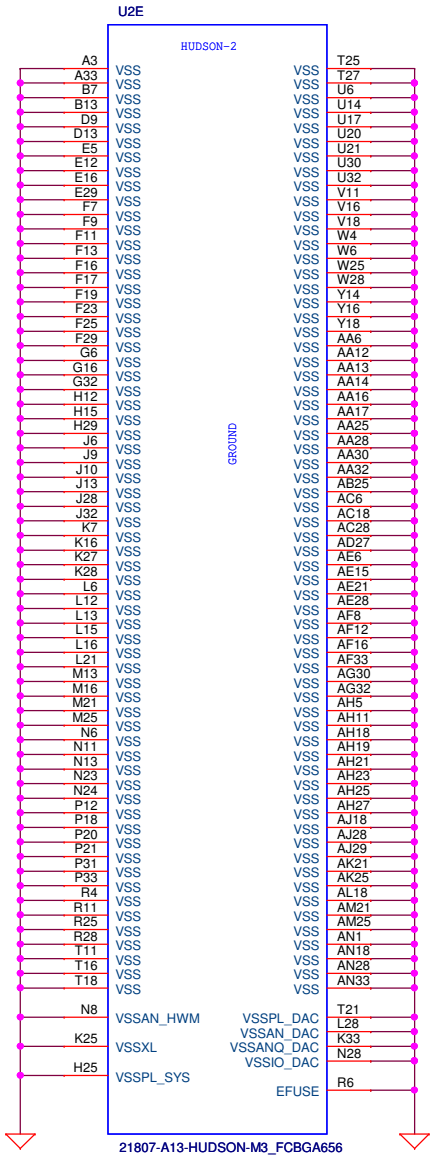
Compal Electronics, Inc.			
Title: FCH-PWR			
Size: Custom	Document Number: ZAMB0		Rev: 0.1
Date: Friday, March 07, 2014	Sheet 24 of 50		



Hud@

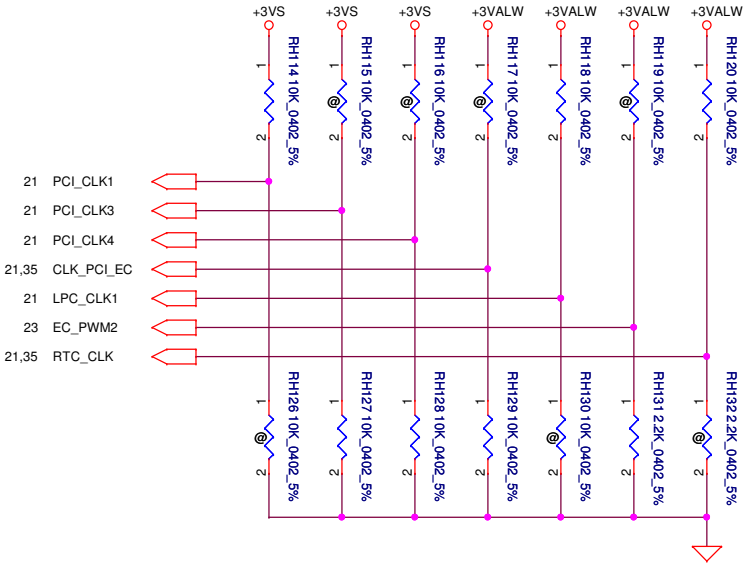
STRAP PINS

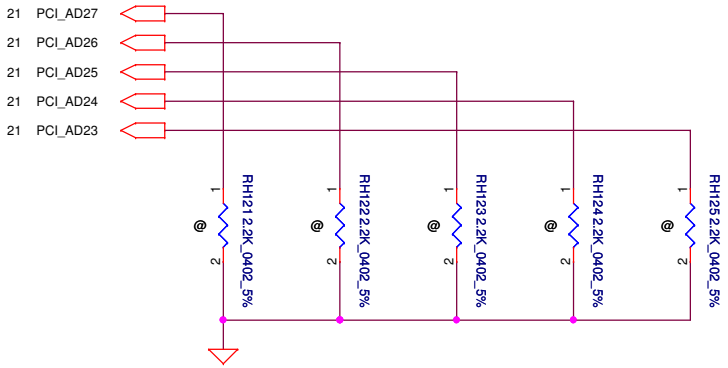
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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Issued Date	2012/09/11	Deciphered Date	2015/07/08

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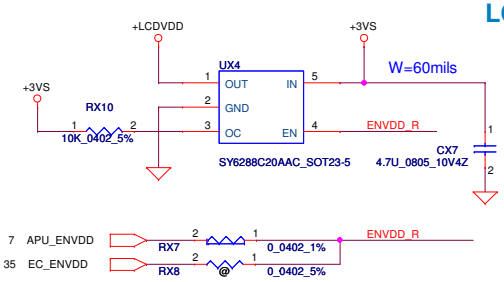
Compal Electronics, Inc.

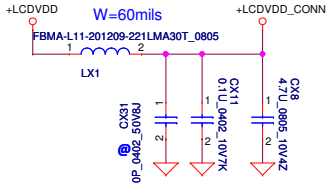
Title: FCH-VSS/Strap

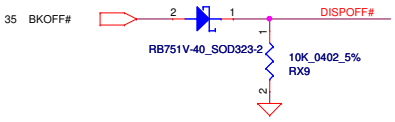
Size: B | Document Number: ZAMB0 | Rev: 0.1

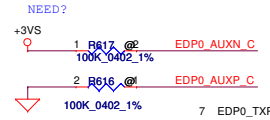
Date: Friday, March 07, 2014 | Sheet 25 of 50

LCD PWR CTRL

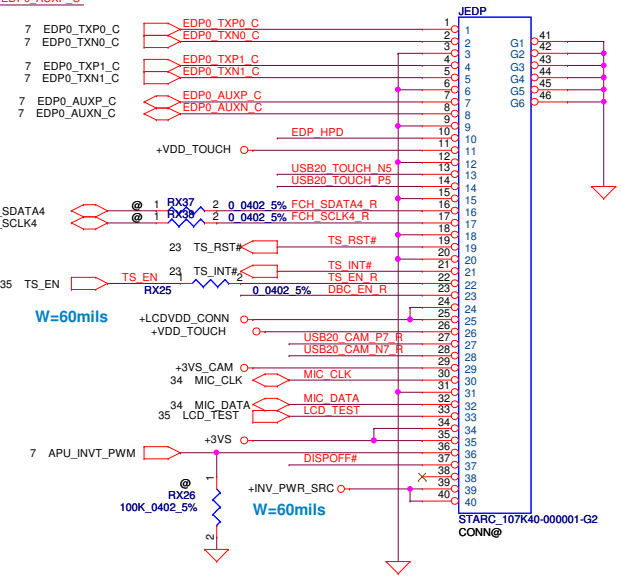


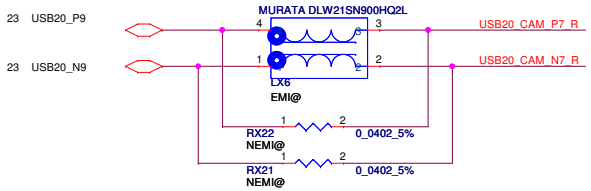


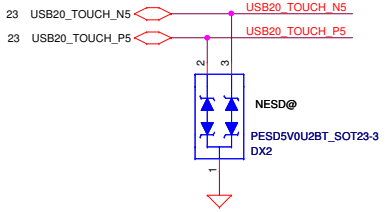




eDP Connector



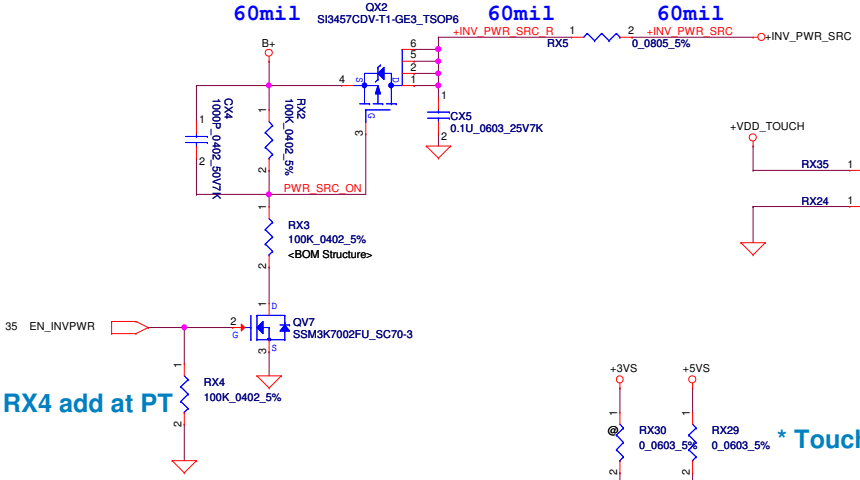




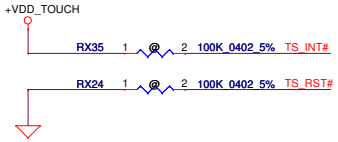
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

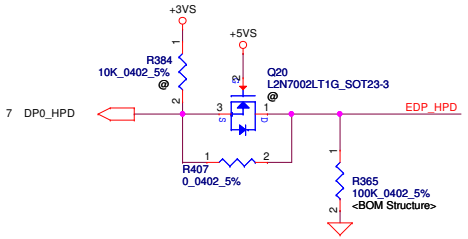
SS table

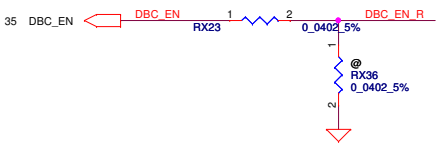
LCD backlight PWR CTRL

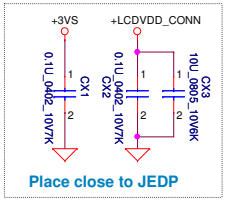


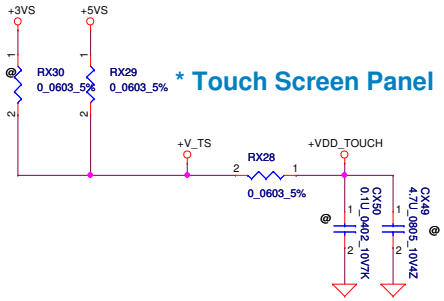
RX4 add at PT

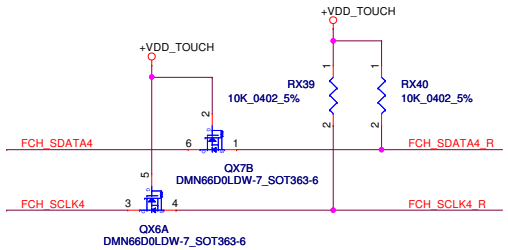




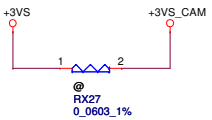








Webcam PWR CTRL



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Compal Electronics, Inc.

Title: CRT Connector.

Size	Document Number	Rev
Custom	ZAMB0	0.1

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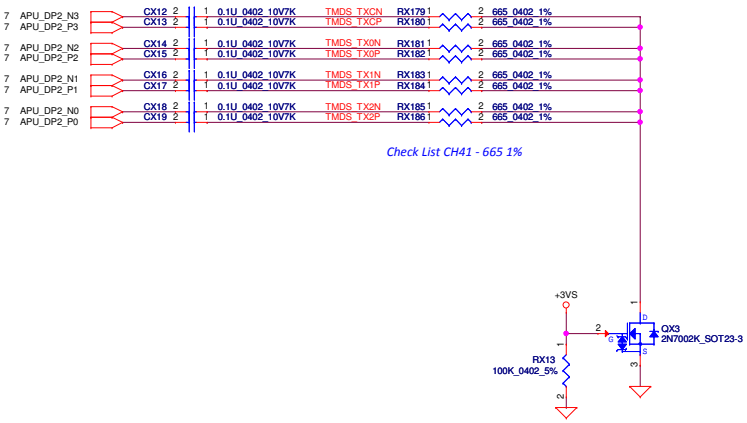

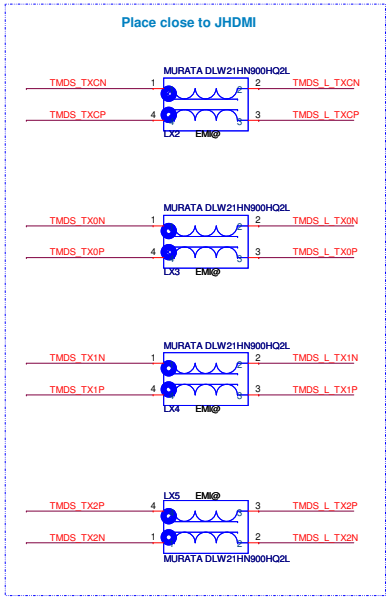

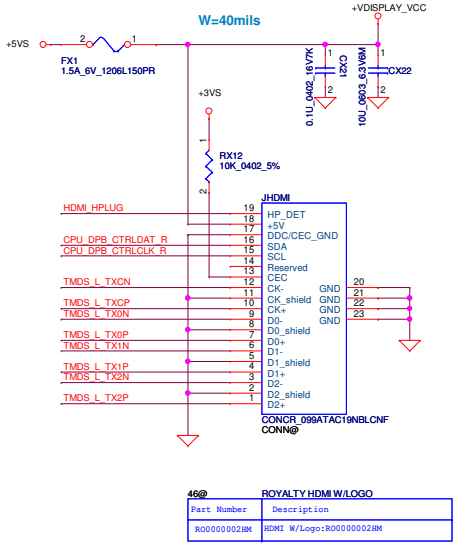

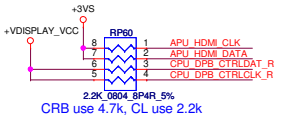

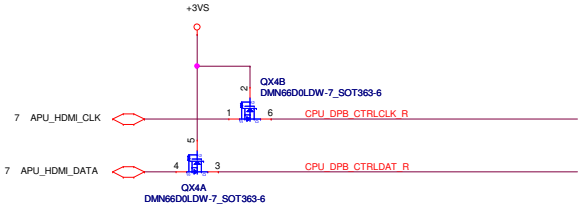

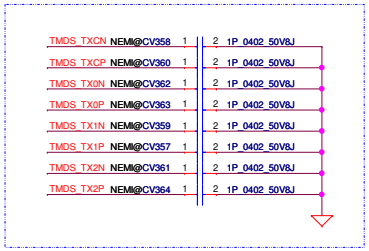

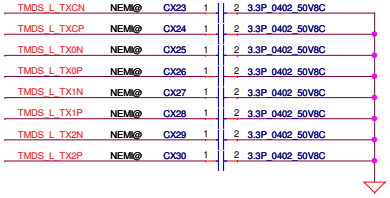

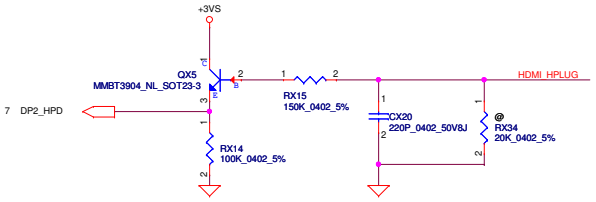

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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: HDMI

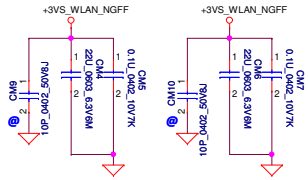
Size | Document Number: ZAMB0 | Rev: 0.1

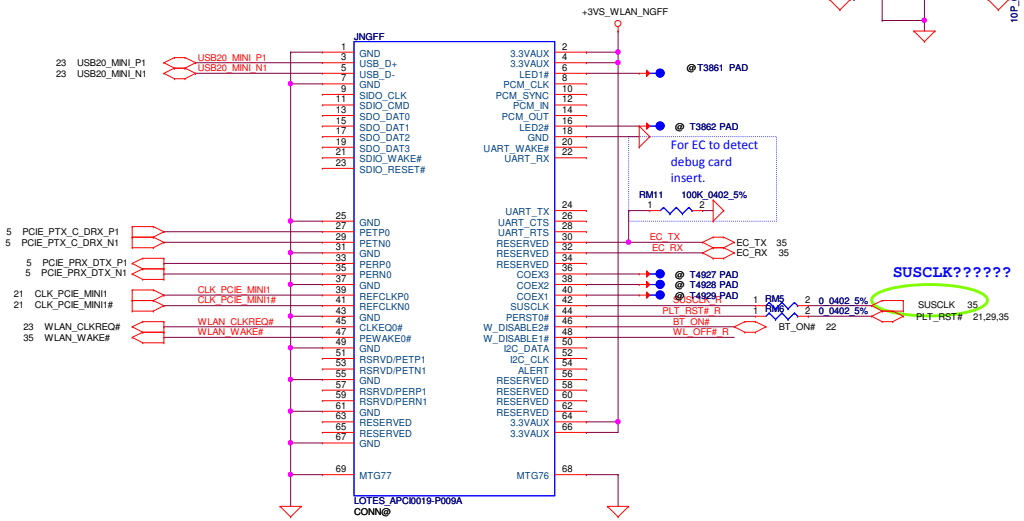
Date: Friday, March 07, 2014 | Sheet 27 of 50

NGFF WL Con (E Key)

closed to pin 2, 4

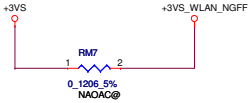
closed to pin 64, 66

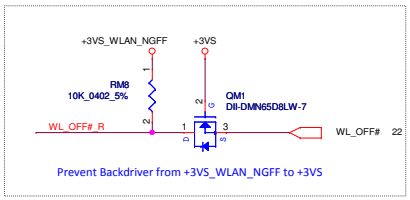




SUSCLK??????

+3VALW TO +3VS_WLAN_NGFF





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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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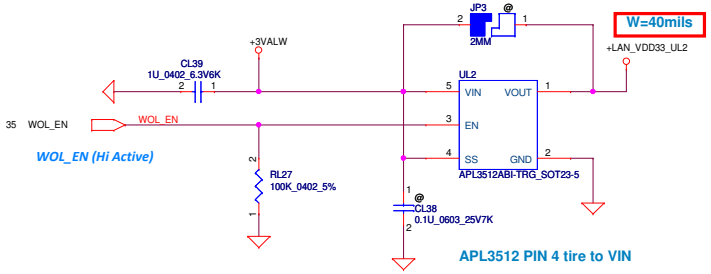
Compal Electronics, Inc.			
Title: NGFF WLAN			
Size	Document Number: ZAMB0		Rev: 0.1
Date: Friday, March 07, 2014	Sheet 28 of 50		

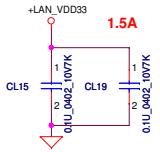
+LAN_IO rising time : >1ms and <100ms

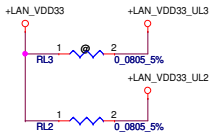
W=40mils



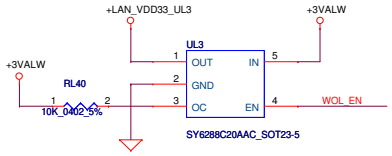
APL3512 PIN 4 tire to VIN

W=40mils

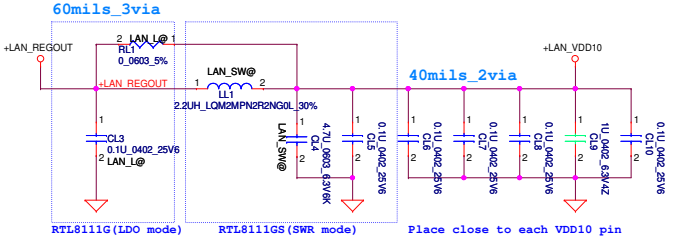


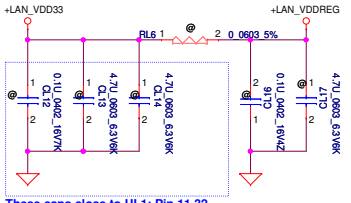


W=40mils

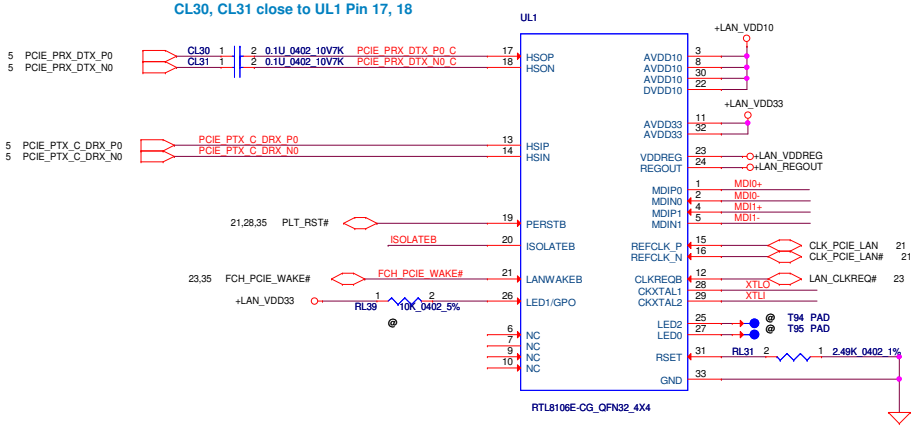


LAN BOM need to confirm

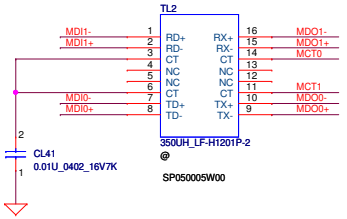


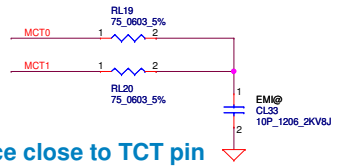


CL30, CL31 close to UL1 Pin 17, 18

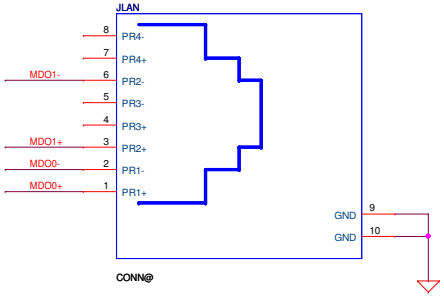


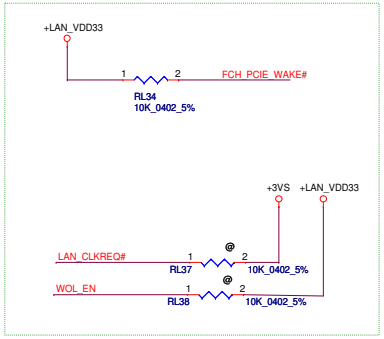
PT use 1TL2

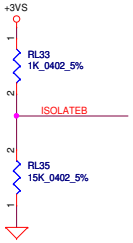




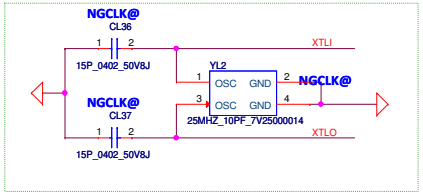
Place close to TCT pin





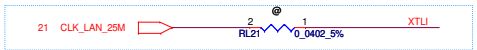


Reserve 10K pull LAN_IO



XTAL

For GCLK



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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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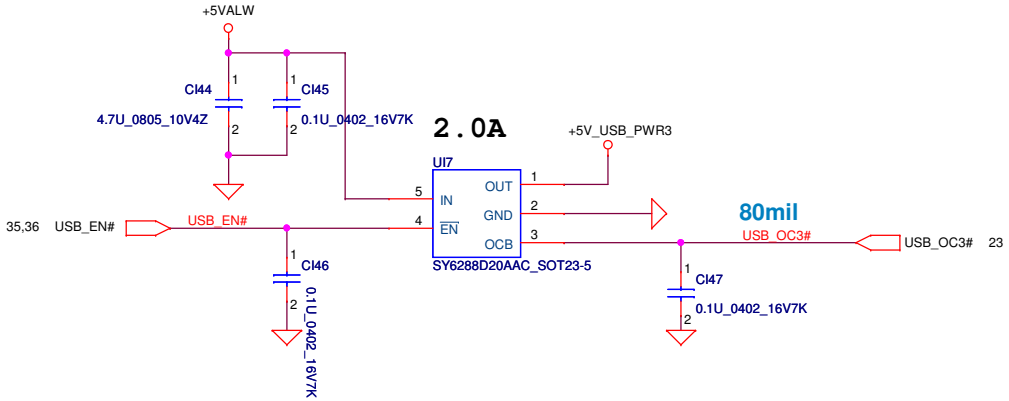
Compal Electronics, Inc.

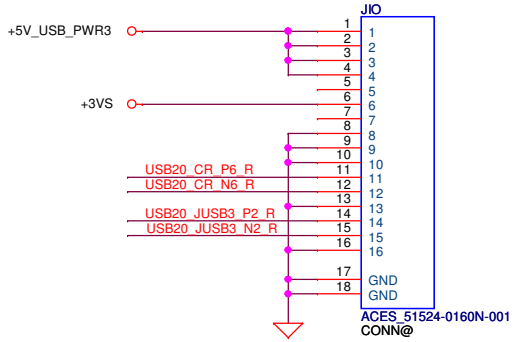
Title: LAN RTL8106EUS

Size: Custom | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 29 of 50

IO to MB CONN
Substitute:SP01001FS00

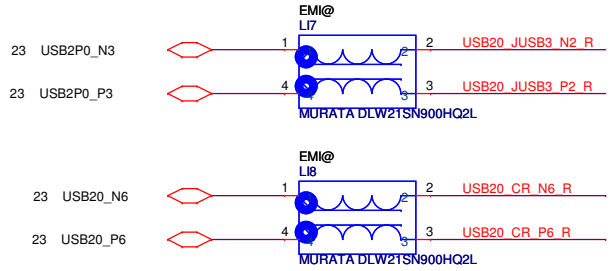




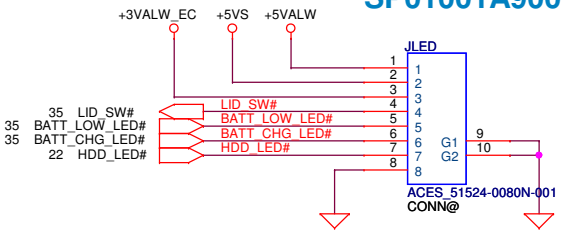
USB Conn

DEBUG Port

Card Reader



LED/B TO M/B
SP01001A900



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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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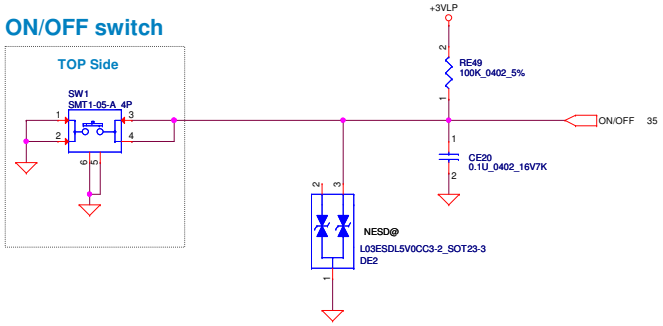
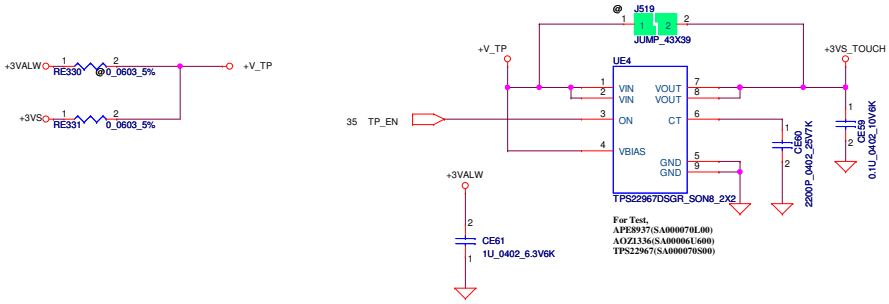
Title	IO/B, LED/B		
Size B	Document Number ZAMB0		Rev 0.1
Date: Friday, March 07, 2014	Sheet 30 of 50		

Power ON Circuit

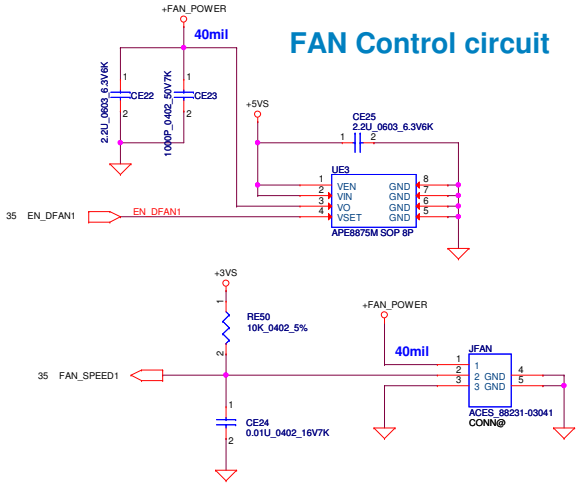
ON/OFF switch



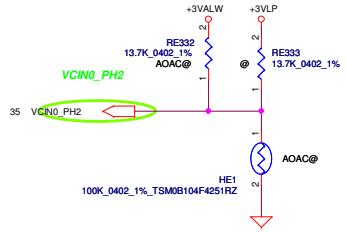
J519 short



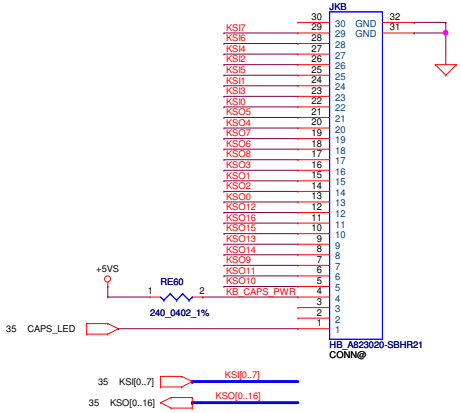
FAN Control circuit



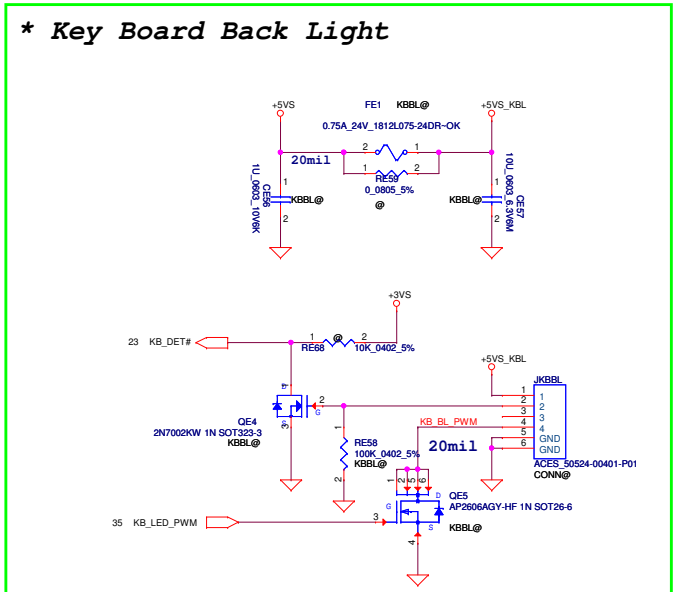
HE1 place around FAN area.



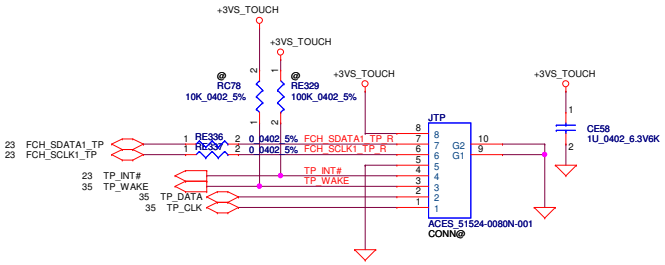
INT_KBD Connector



* Key Board Back Light



Touch pad PS/2 only



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 31 of 50

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/12	Deciphered Date	2015/07/08

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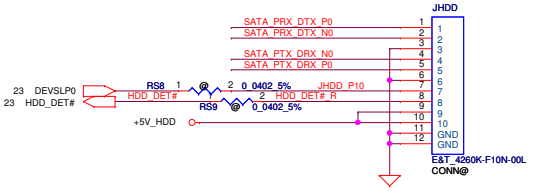
Title: SMSC thermal sens/FAN/screw

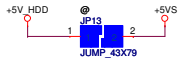
Size	Document Number	Rev
Custom	ZAMB0	0.1

Date: Friday, March 07, 2014 Sheet 32 of 50

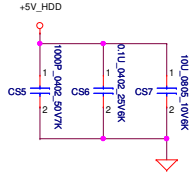
SATA HDD Connector

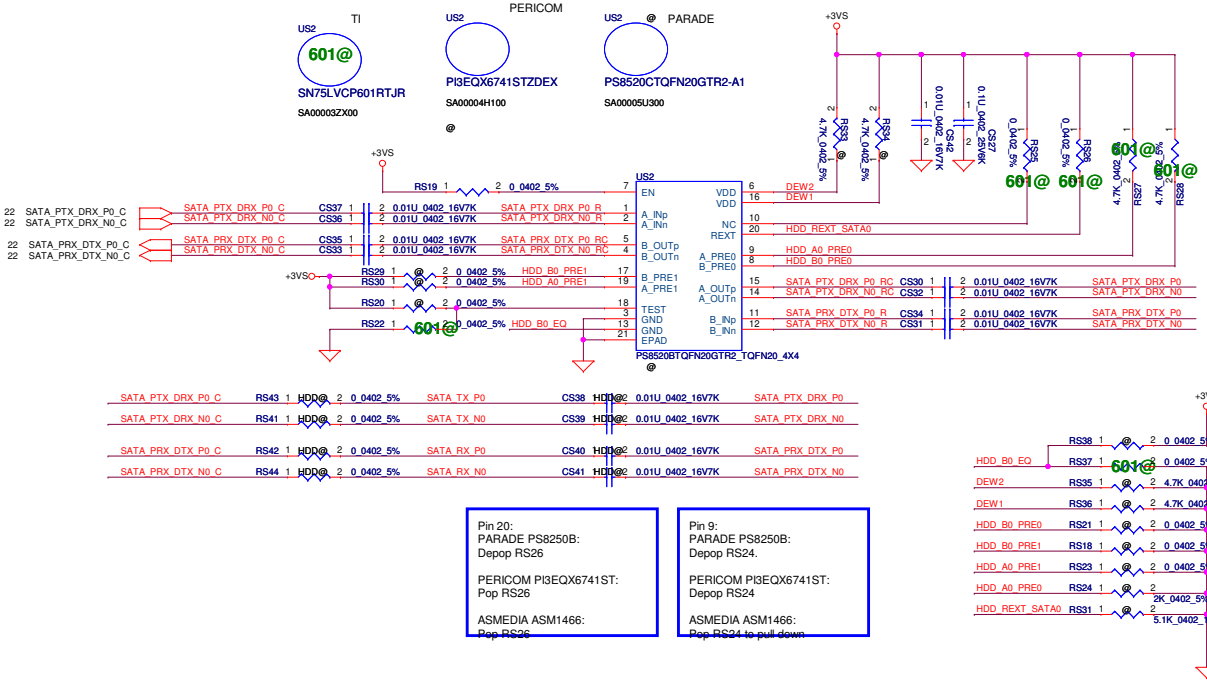


+5V_HDD Source



SHORT DEFAULT





Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: HDD

Size | Document Number: ZAMB0 | Rev: 0.1

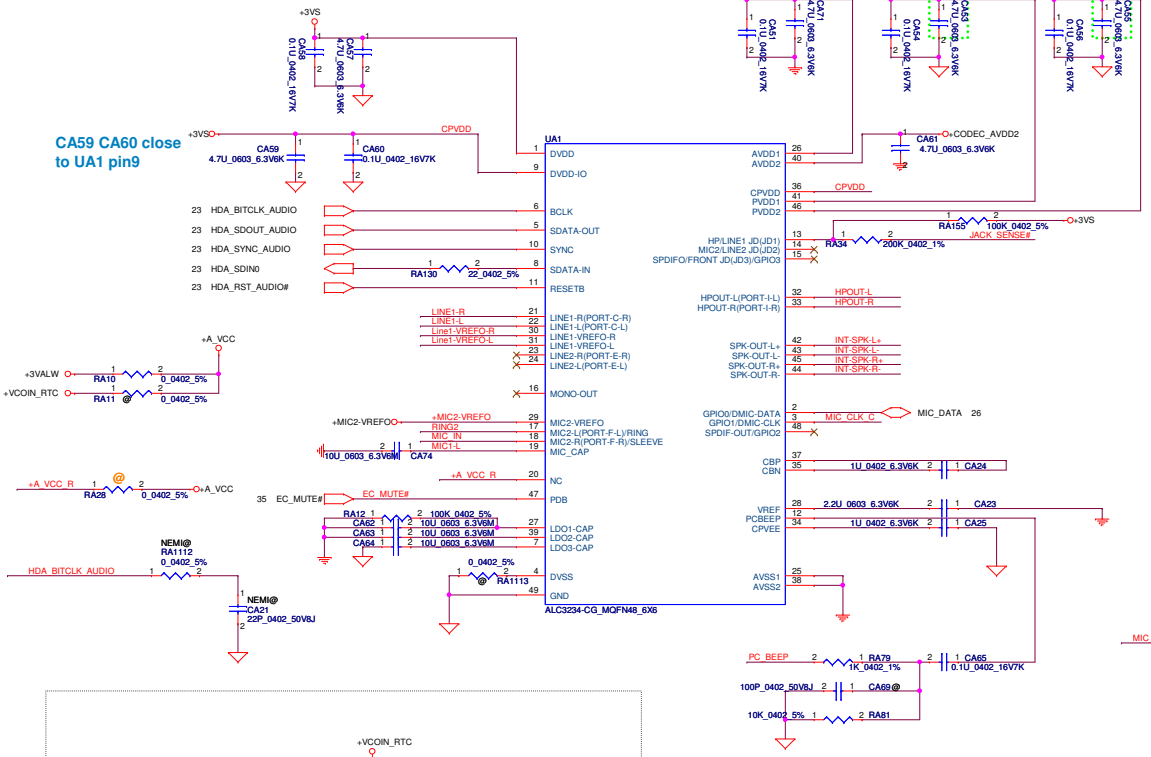
Date: Friday, March 07, 2014 | Sheet 33 of 50

CA71, CA51 place close to Pin 26

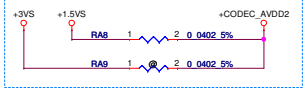
CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

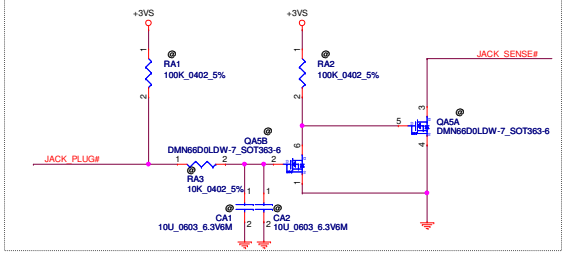
CA59 CA60 close to UA1 pin9



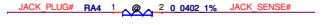
Reserve for HDA issue



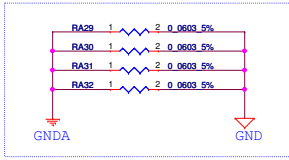
JACK_PLUG Delay circutis



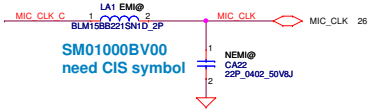
Reserve for cancel Delay circutis

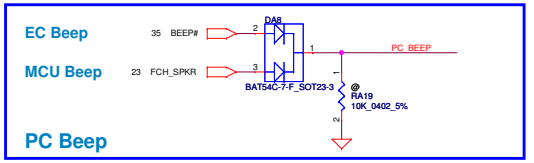


Place on the moat between GND & GNDA.



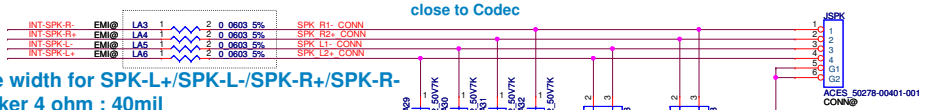
SM01000BV00
need CIS symbol



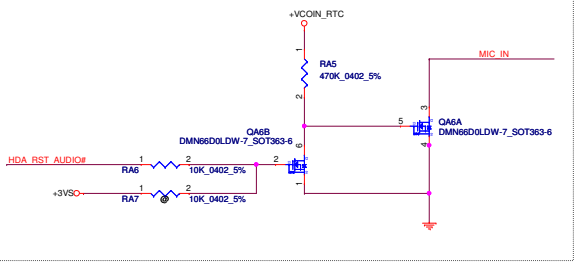


Close to UA1 Pin11,13,14,16

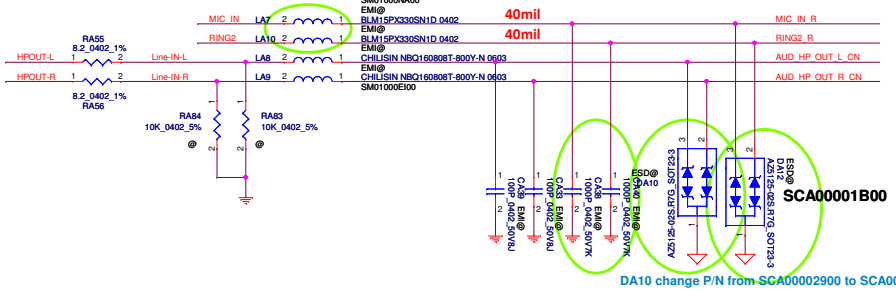
close to Codec



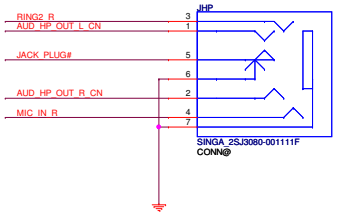
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



iPhone and Nokia type Combo Jack



DA10 change P/N from SCA00002900 to SCA00001A00



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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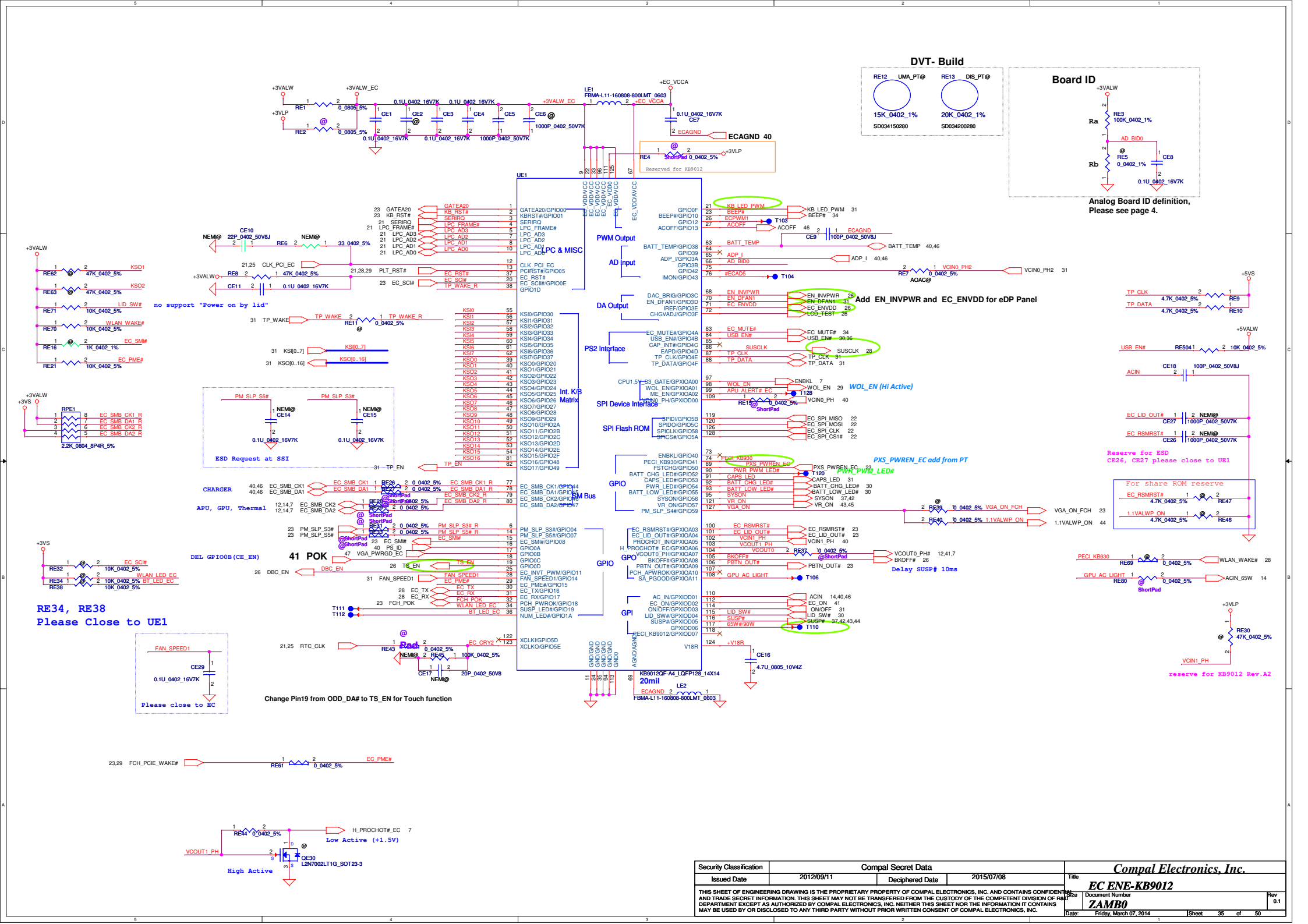
Compal Electronics, Inc.

Title: Audio Codec ALC3234

Size: B | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 34 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2015/07/08

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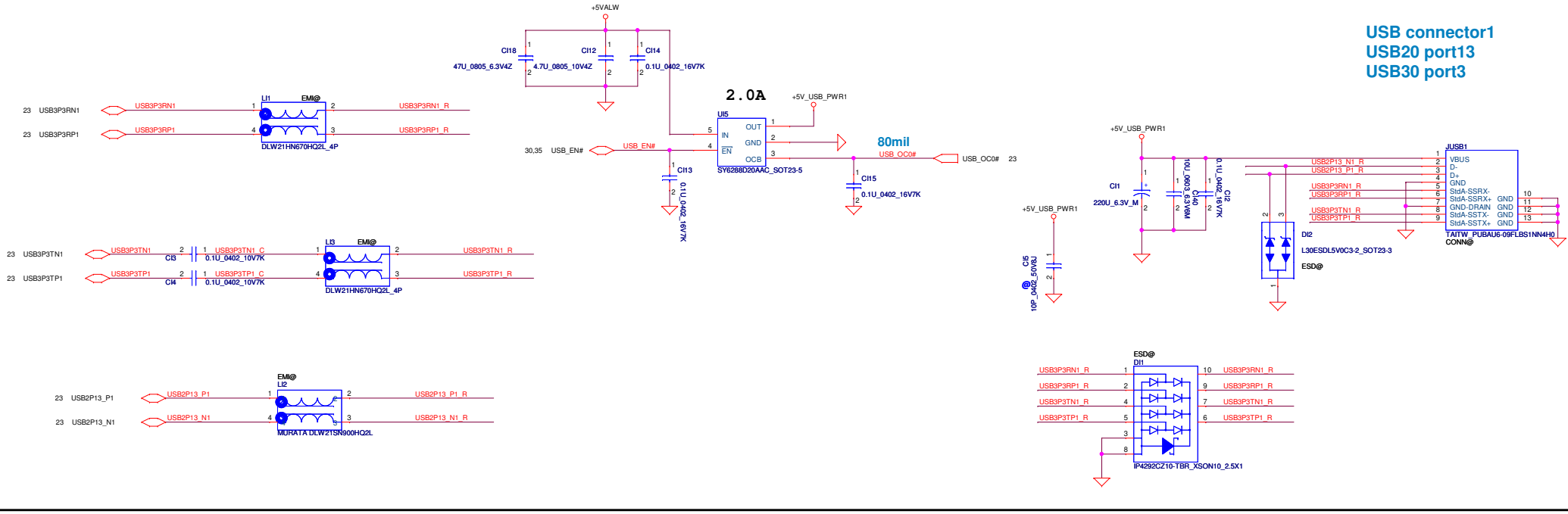
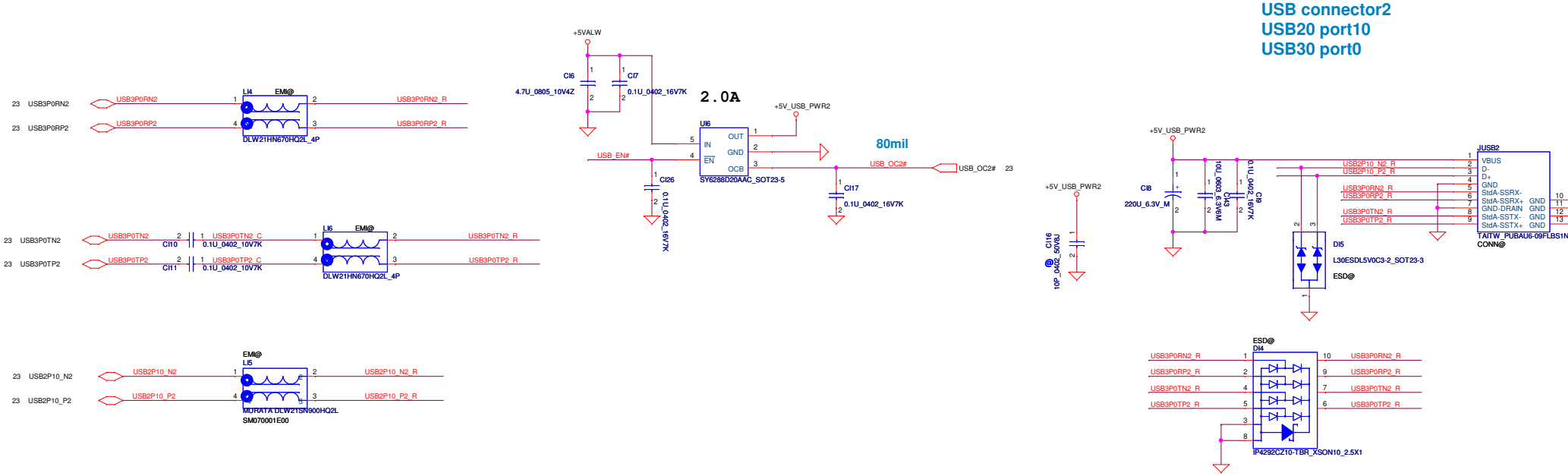
Compal Electronics, Inc.

Title: EC ENE-KB9012

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 35 of 50





Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.	
Title	USB3.0
Size	Document Number: ZAMB0
Rev	0.1
Date:	Friday, March 07, 2014
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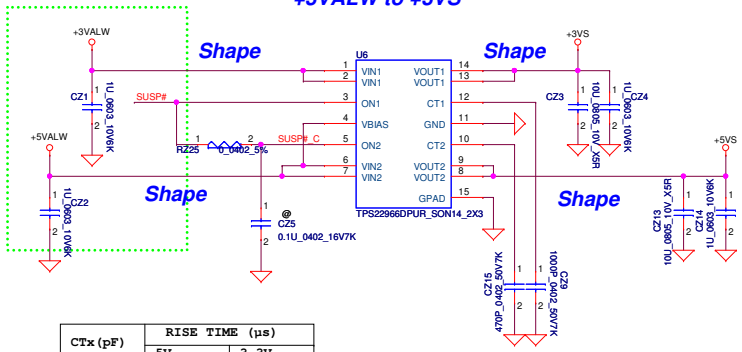
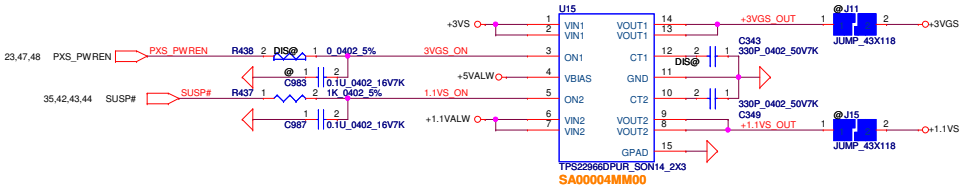
+5VALW to +5VS
+3VALW to +3VS

CZ3, CZ13 Change to H=0.85mm



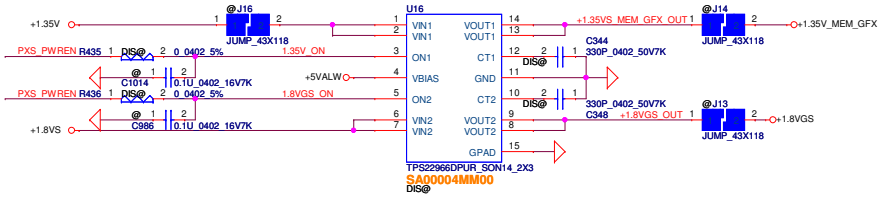
CTx(pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835

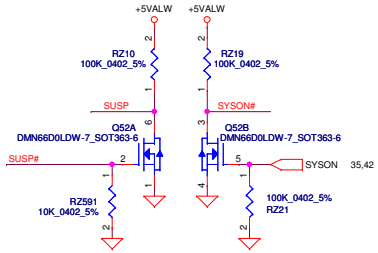
+1.1VALW to +1.1VS
+3VS to +3VGS

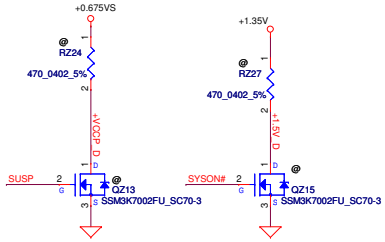


+1.35V to +1.35VS_MEM_GFX_OUT
+1.8VS to +1.8VSDGPU

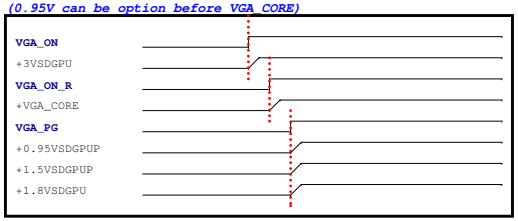
J13 OPEN DEFAULT







VGA sequence : default same as V5WE2
(0.95V can be option before VGA_CORE)



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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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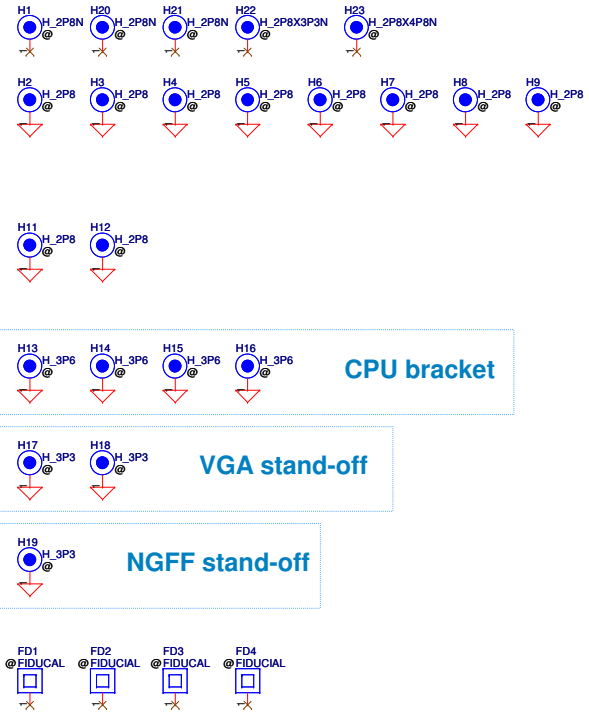
Compal Electronics, Inc.

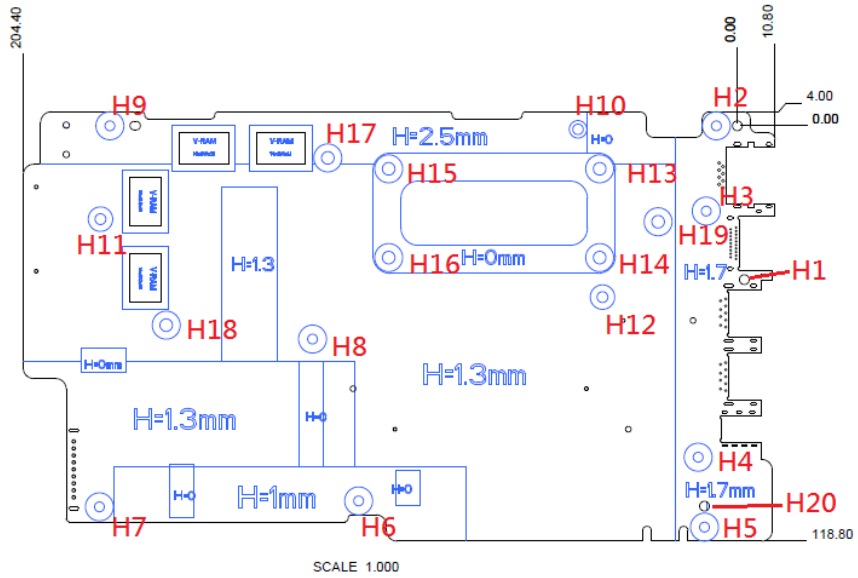
Title: **DC/DC Interface**

Size | Document Number: **ZAMB0** | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 37 of 50

Screw Hole





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Issued Date	2013/10/01	Deciphered Date	2015/07/08

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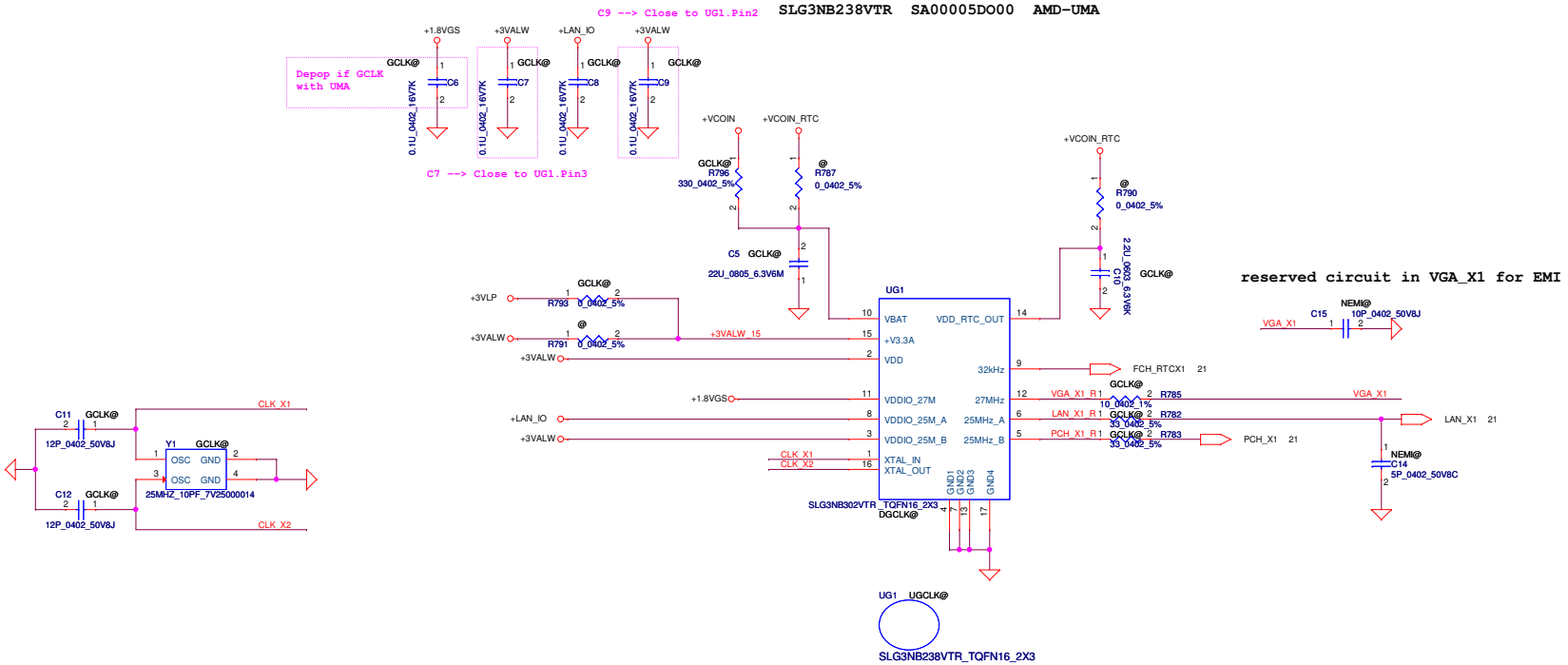
Compal Electronics, Inc.

Title: Screw Hole

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 38 of 50

SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005DO00 AMD-UMA



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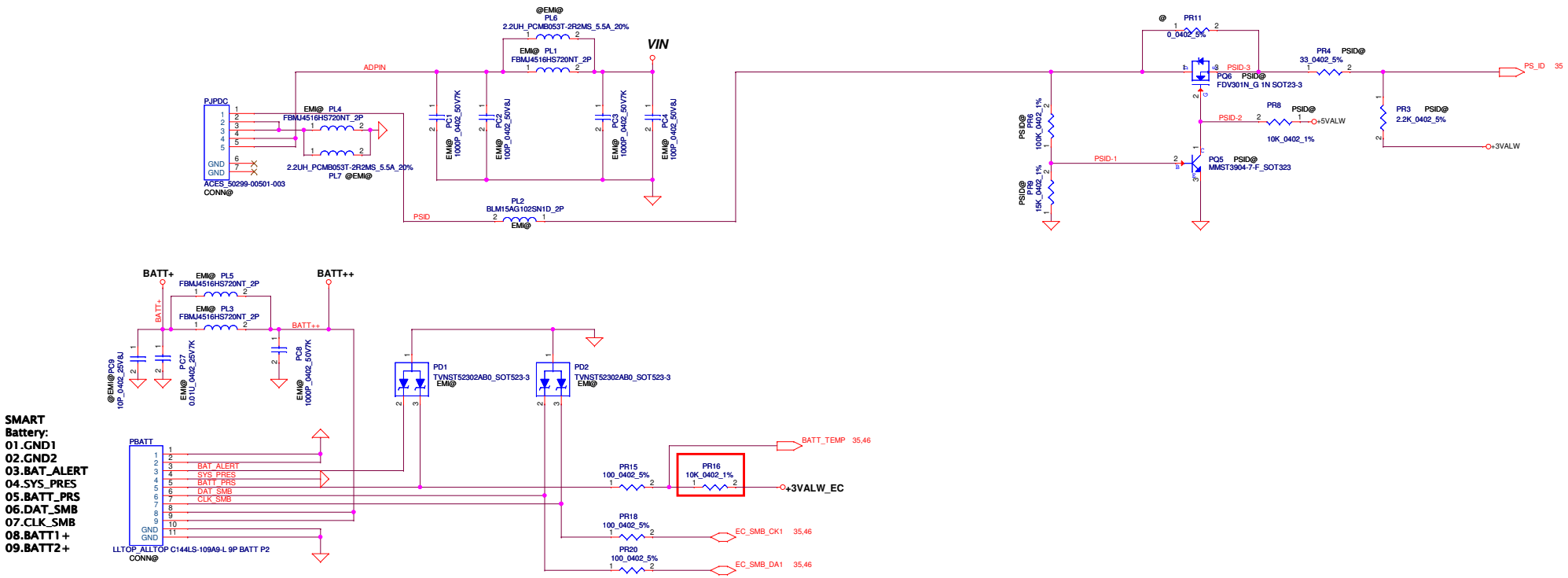
Compal Electronics, Inc.

Title: GCLK

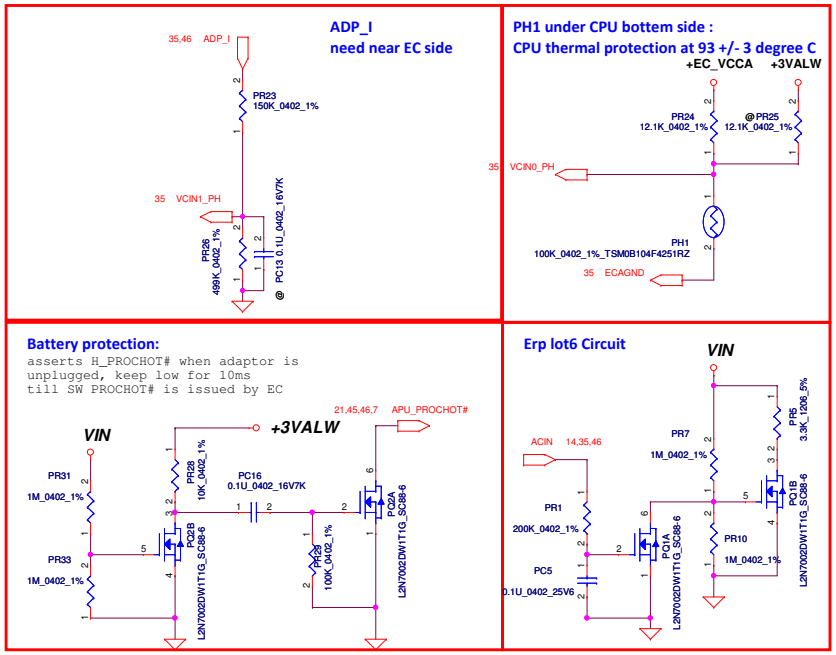
Size | Document Number: ZAMB0 | Rev: 0.1

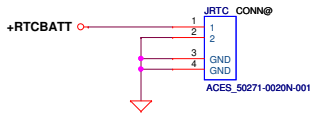
Date: Friday, March 07, 2014 | Sheet 39 of 50



SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)





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Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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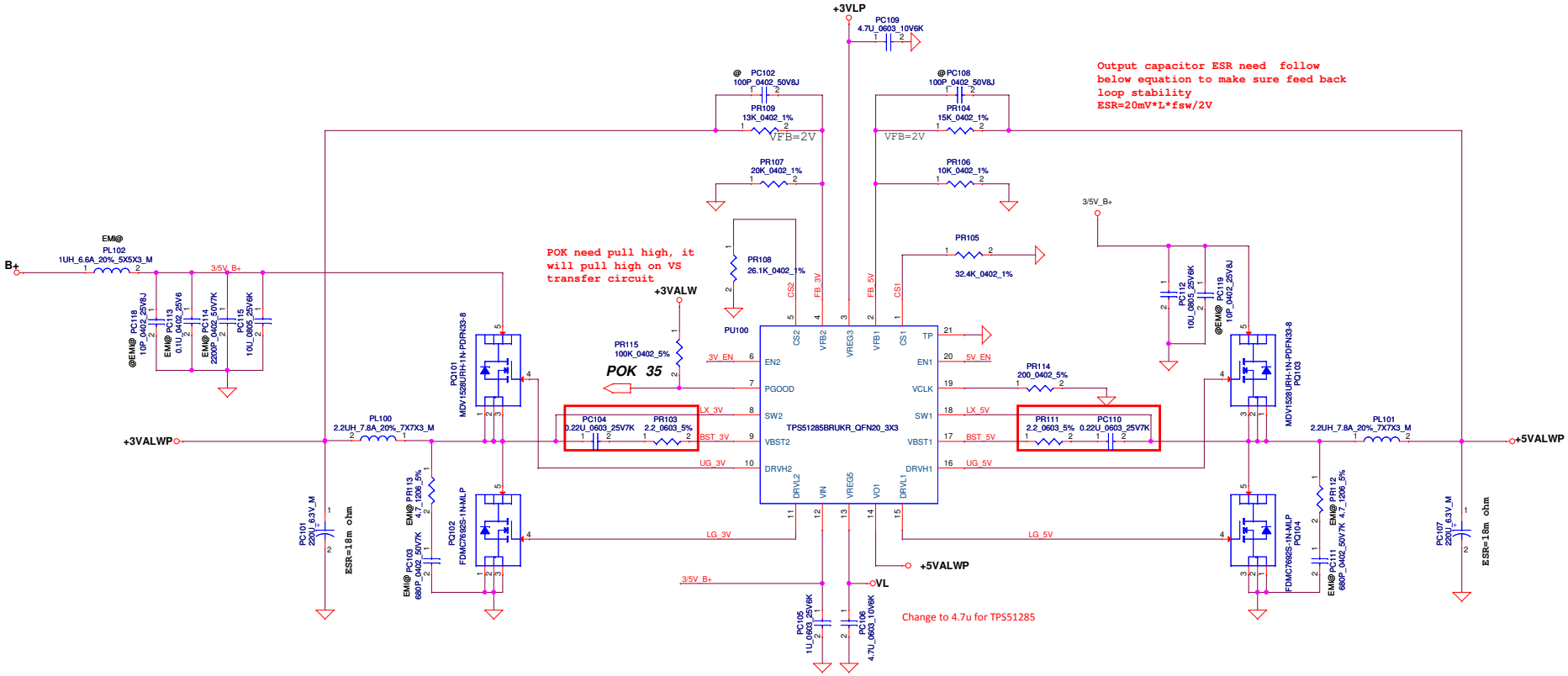
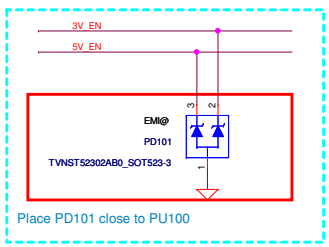
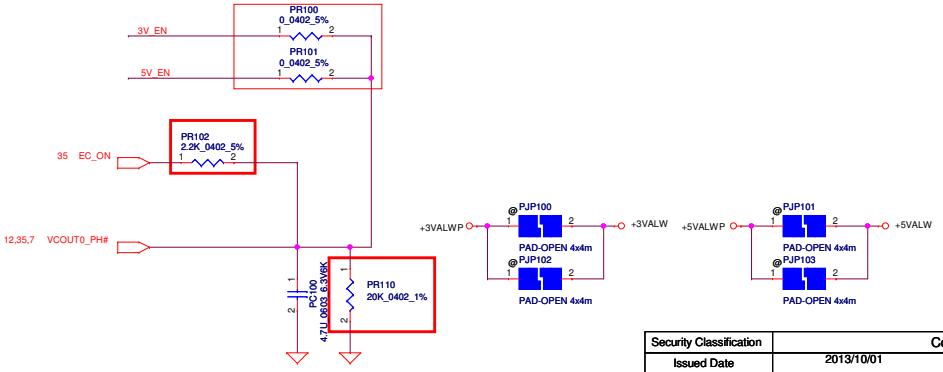
Compal Electronics, Inc.	
Title	PWR_DCIN/BATT CONN/OTP
Size	Document Number: ZAMB0 — Rev: 0.1
Date: Friday, March 07, 2014	Sheet 40 of 50



3VALWP
TDC 7.45A
Peak Current 9.34A
OCP current 11.21A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm





5VALWP
TDC 8A
Peak Current 11.42A
OCP current 13.7A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm

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Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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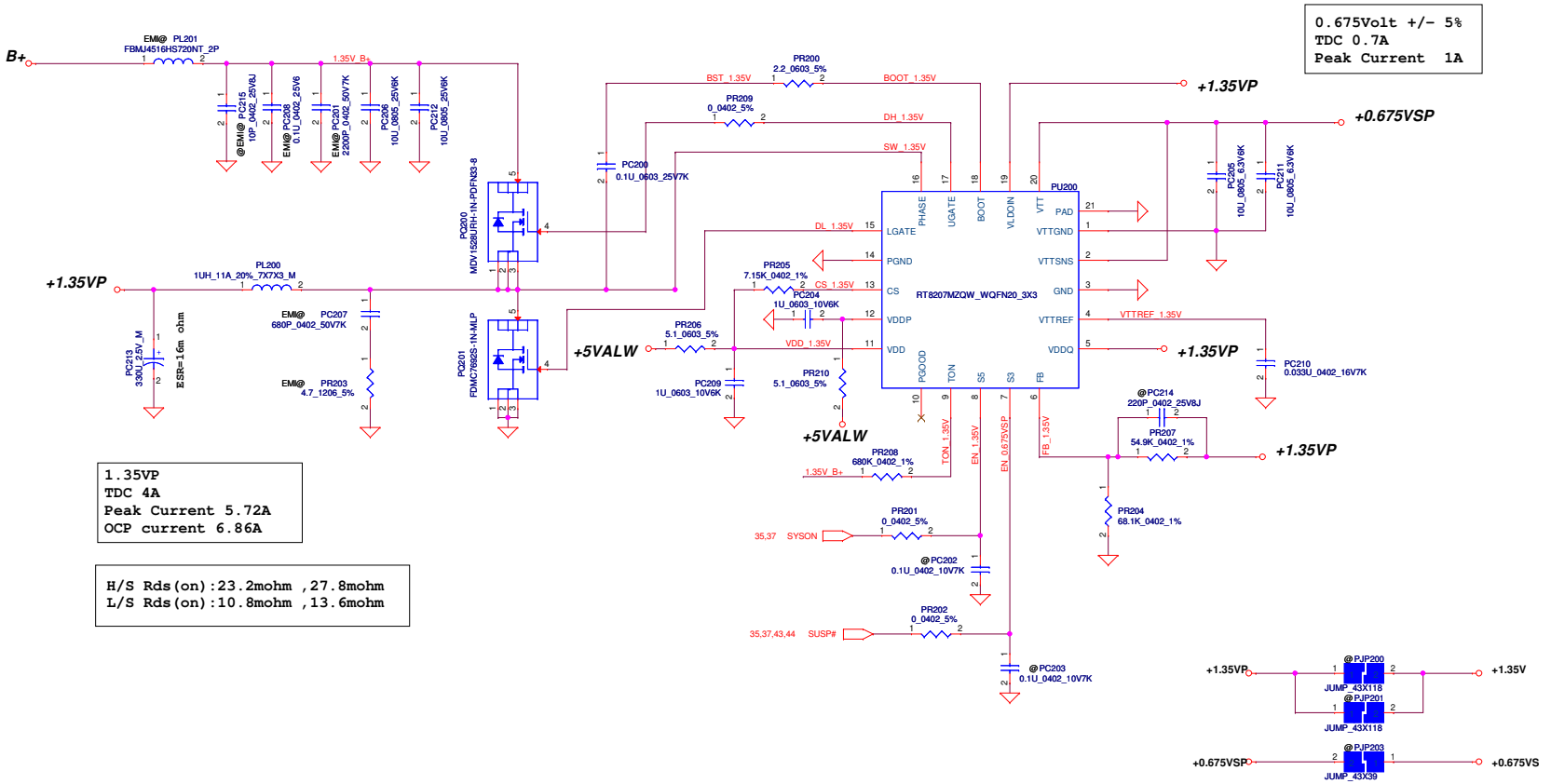
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 41 of 50



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Security Classification	Compal Secret Data		
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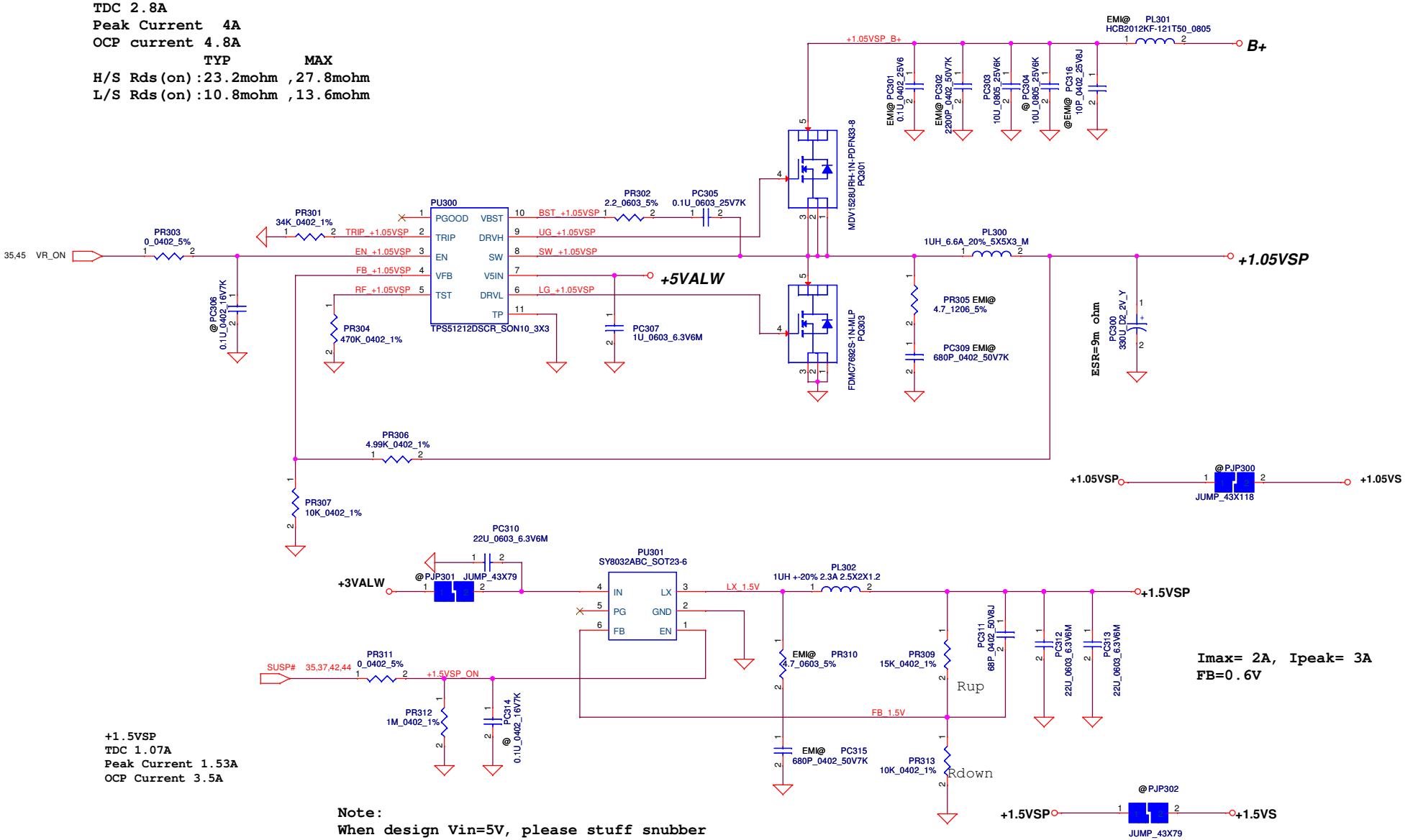
Compal Electronics, Inc.			
Title	PWR_+1.35VP/0.675VSP		
Size	Document Number		Rev
	ZAMB0		0.1
Date:	Friday, March 07, 2014	Sheet 42 of 50	

1.05VSP
TDC 2.8A
Peak Current 4A
OCP current 4.8A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm



Imax= 2A, Ipeak= 3A
FB=0.6V

+1.5VSP
TDC 1.07A
Peak Current 1.53A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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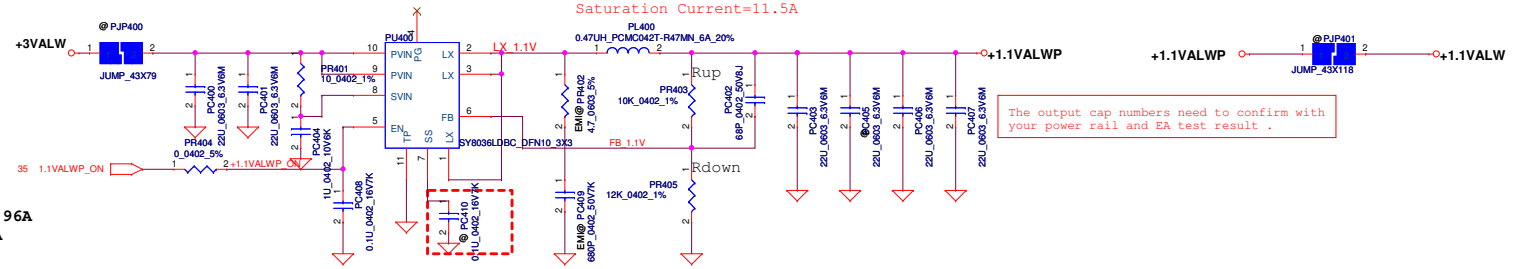
Title	PWR_+1.05VSP_+1.5VSP		
Size	Document Number ZAMB0		Rev 0.1
Date: Friday, March 07, 2014		Sheet 43 of 50	

FB=0.6V
Note:Iload(max)=6A

4*4 DCR 14~15.5mΩ
Heat Rating Current=6A
Saturation Current=11.5A



1.1VALWP
TDC 3.47A
Peak Current 4.96A
OCP current 7.5A

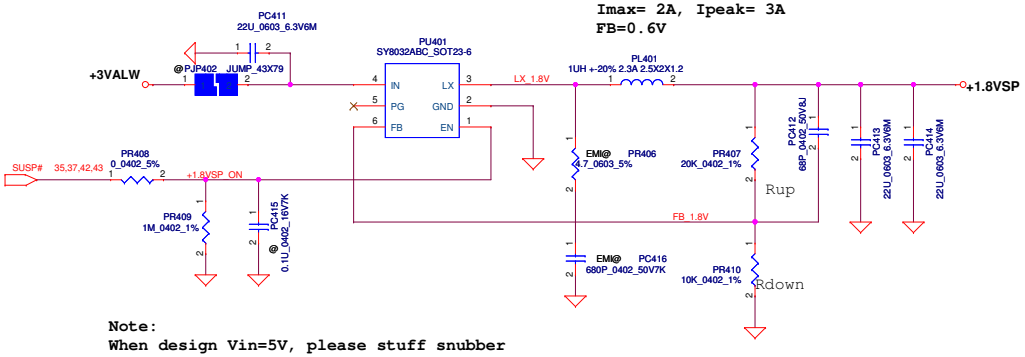
Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

PC7 to set the Soft Start Time:
CSS=100nF 6ms
Without CSS 0.6ms

Vout=0.6V* (1+Rup/Rdown)

Over voltage IC latch off protection threshold
min=115% type=120% max=125 %
Delay time 10us

Imax= 2A, Ipeak= 3A
FB=0.6V



+1.8VSP
TDC 1.34A
Peak Current 1.92A
OCP Current 3.5A

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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Issued Date	2013/10/01	Deciphered Date 2015/07/08	Title: PWR_+1.1ALWP / +1.8VSP
Size	Document Number: ZAMB0		Rev: 0.1
Date: Friday, March 07, 2014	Sheet 44 of 50		

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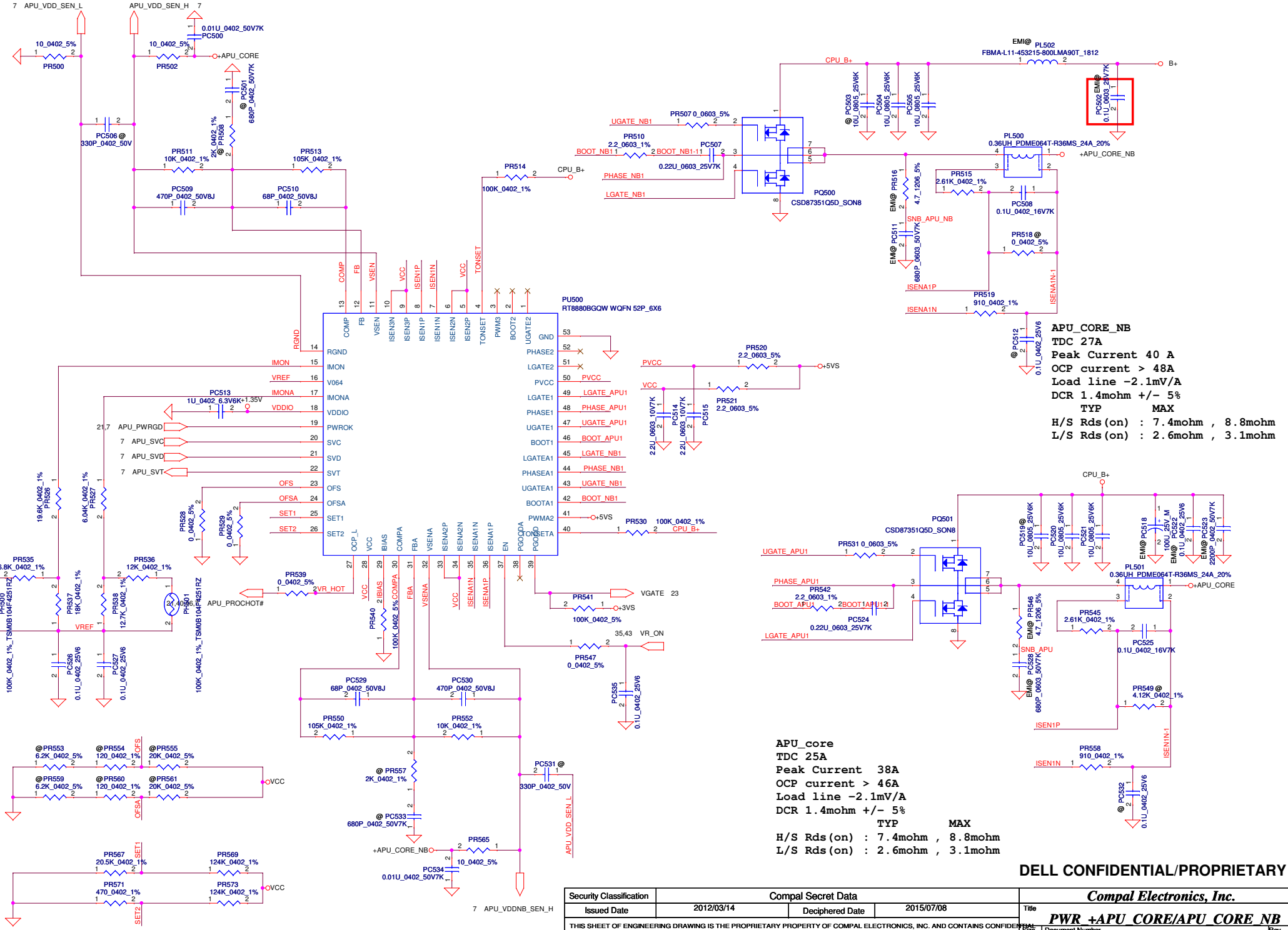

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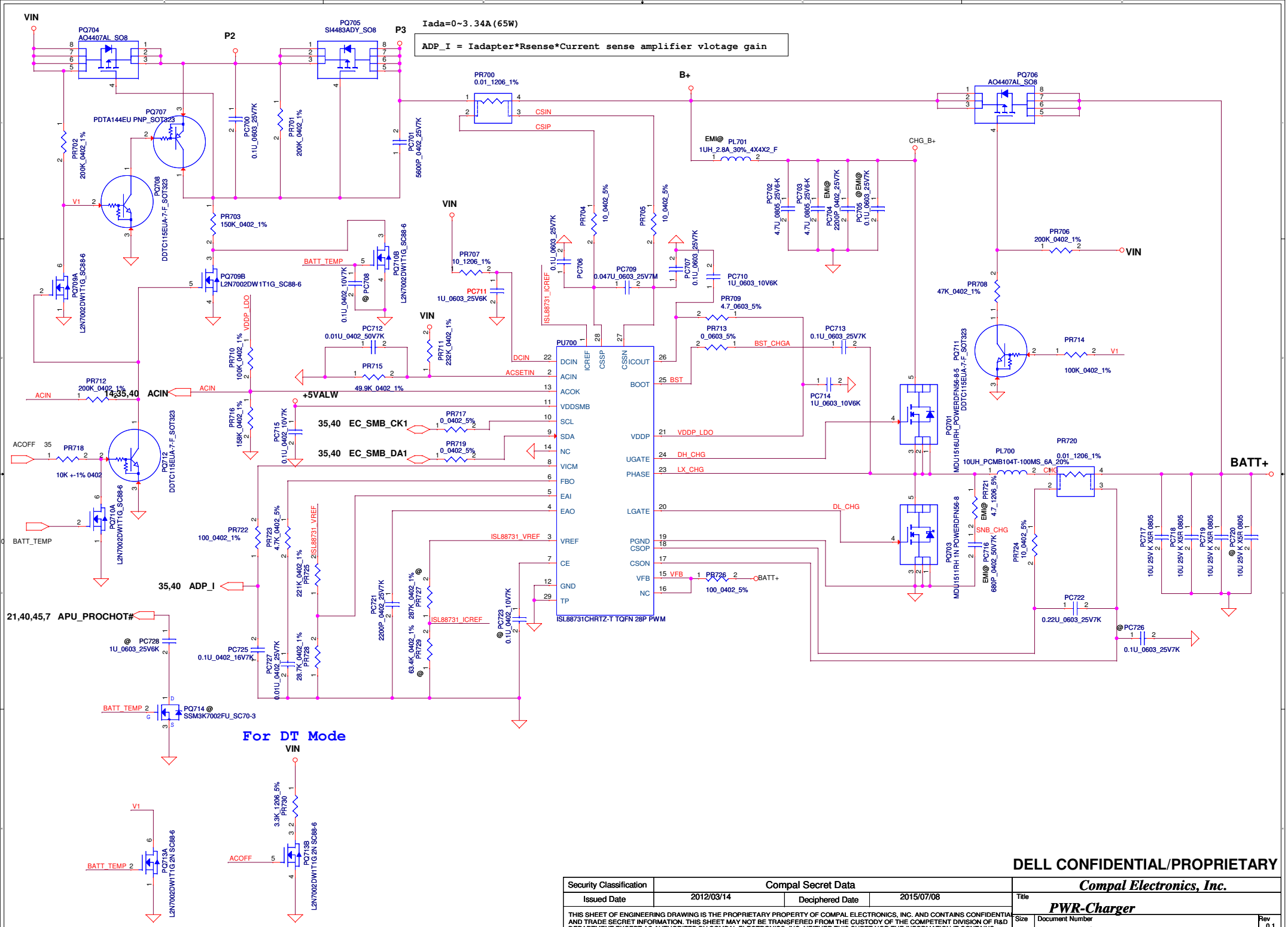
Compal Electronics, Inc.

Title: PWR_+APU_CORE/APU_CORE_NB

Size: B | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 45 of 50


Iada=0~3.34A(65W)
ADP_I = Iadapter*Rsense*Current sense amplifier vlotage gain
VIN
B+
BATT+
CHG_B+
+5VALW
ACIN
ACOFF
BATT_TEMP
ISL88731_VREF
ISL88731_ICREF
VDDP_LDO
DCIN
ACSETIN
BST_CHGA
DH_CHG
LX_CHG
DL_CHG
SNB_CHG
CSIN
CSIP
VFB
BST
ICOUT
VDDSMB
EC_SMB_CK1
EC_SMB_DA1
ADP_I
APU_PROCHOT#
PU700
ISL88731CHRTZ-T TQFN 28P PWM
For DT Mode
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Compal Electronics, Inc.
PWR-Charger
ZAMB0
Security Classification
Compal Secret Data
Issued Date
2012/03/14
Deciphered Date
2015/07/08
Friday, March 07, 2014
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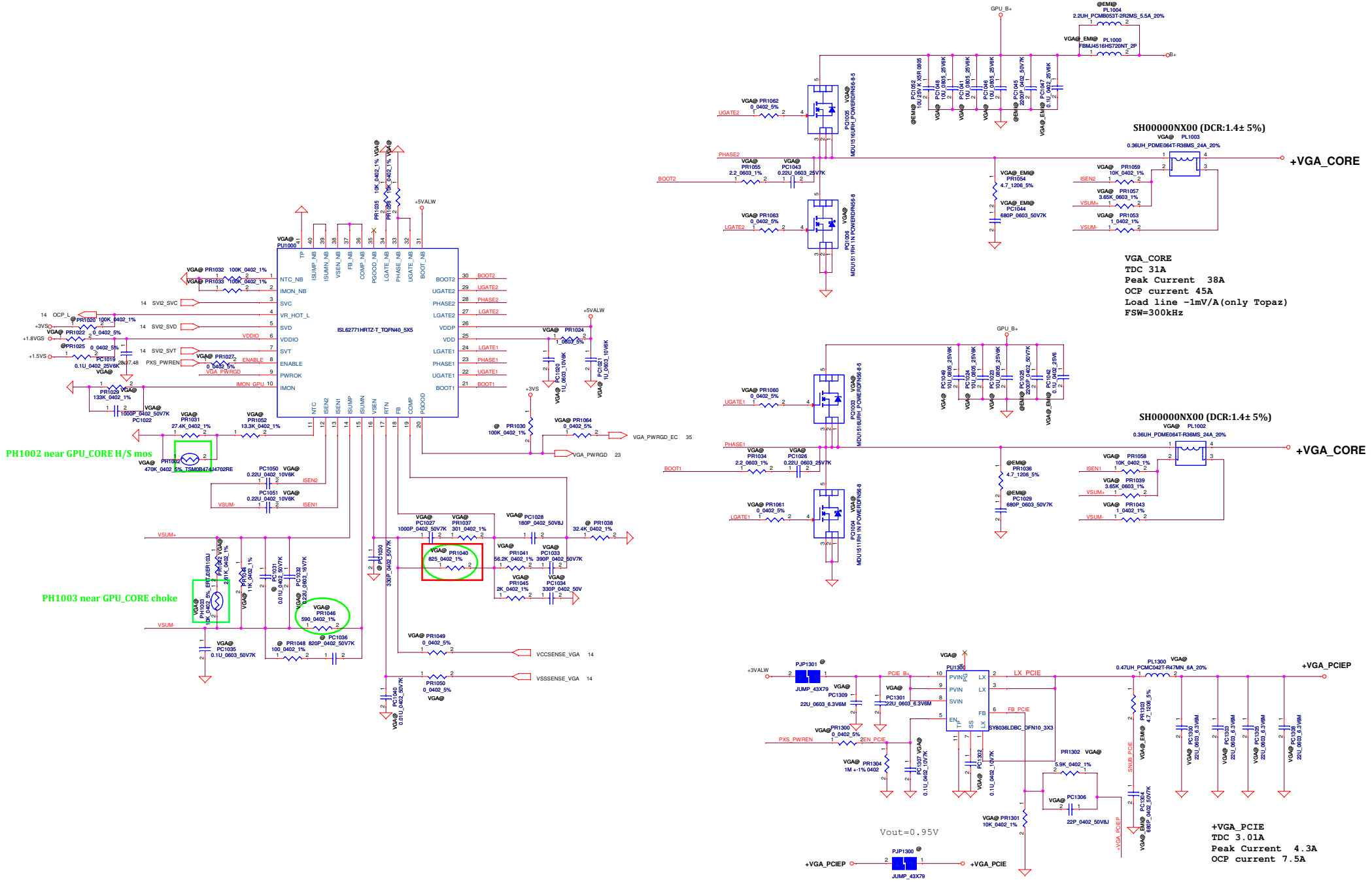

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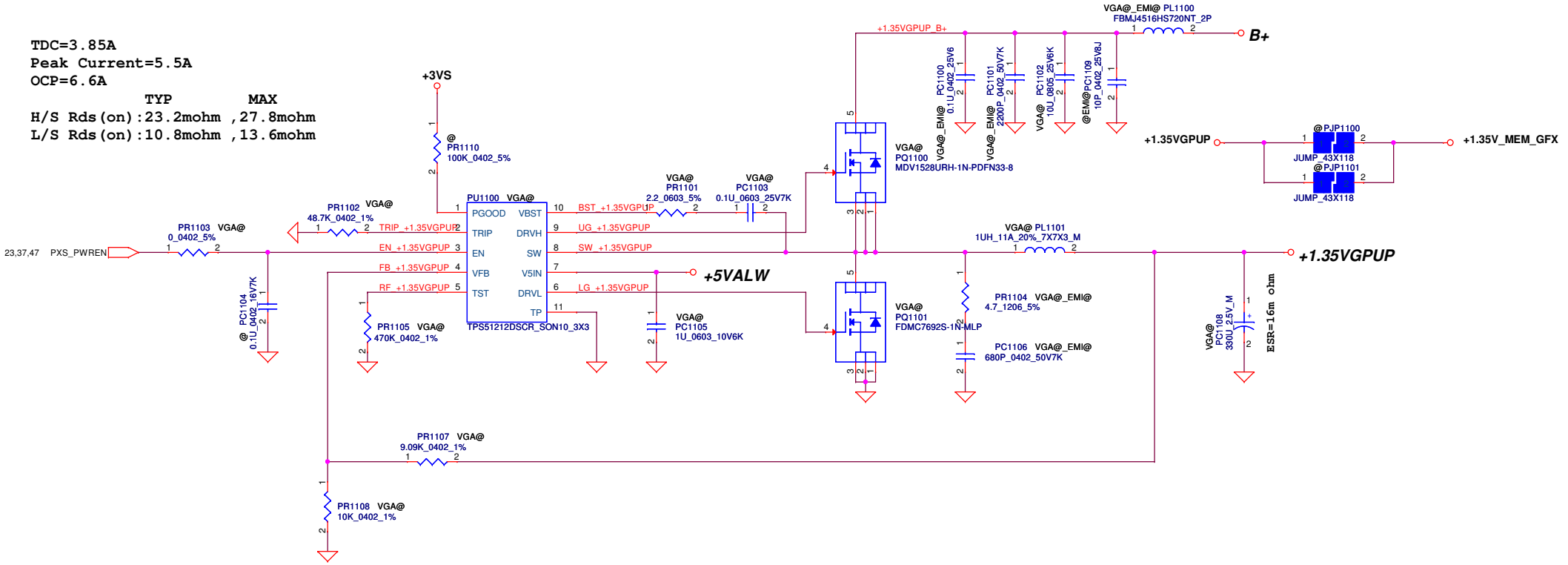
TDC=3.85A
Peak Current=5.5A
OCP=6.6A

	TYP	MAX
H/S Rds(on)	23.2mohm	27.8mohm
L/S Rds(on)	10.8mohm	13.6mohm



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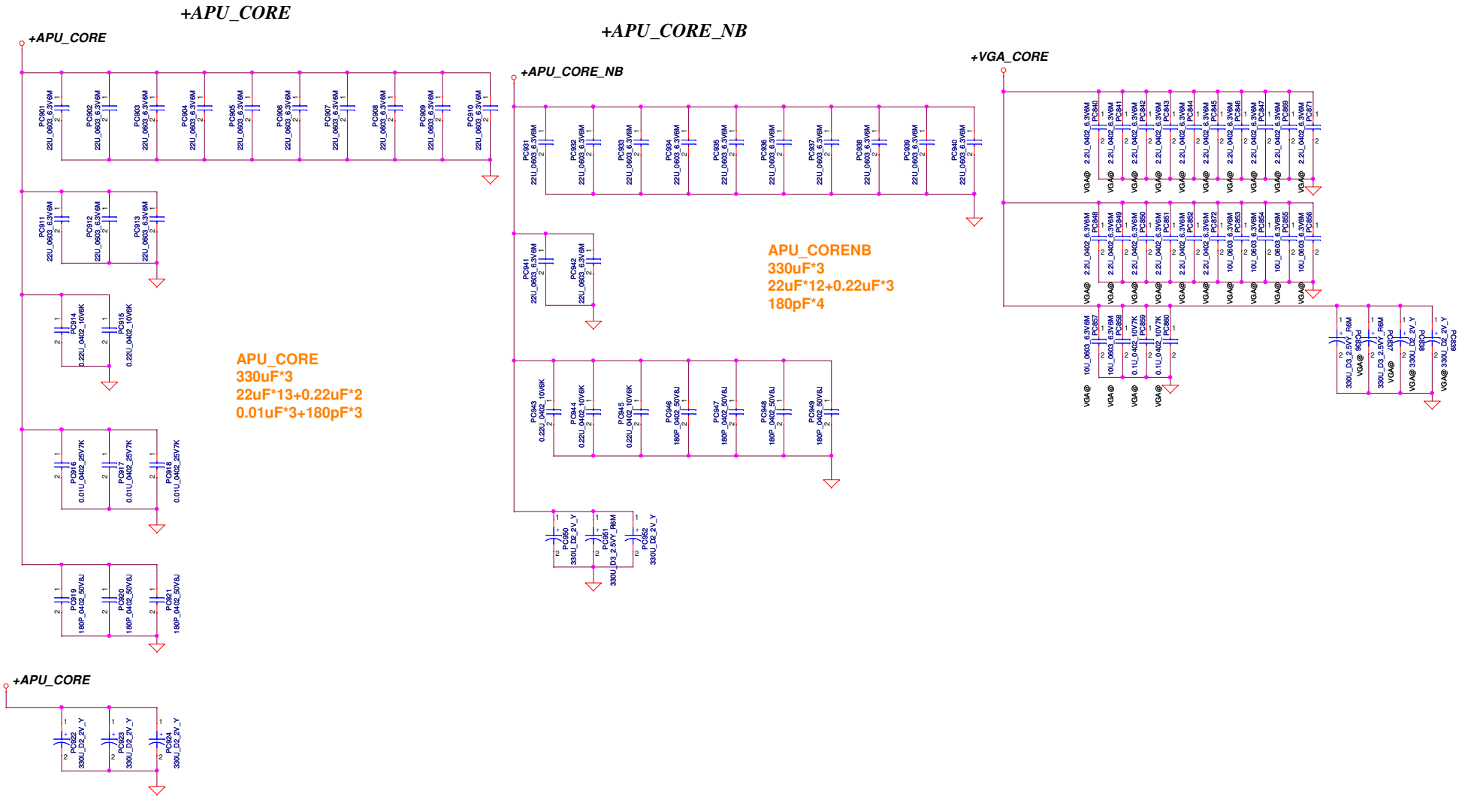
Compal Electronics, Inc.

Title: PWR_+1.35VGPU

Size | Document Number: ZAMB0 | Rev: 0.1

Date: Friday, March 07, 2014 | Sheet 48 of 50



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Issued Date	2013/10/01	Deciphered Date 2015/07/08	Title: PWR_PROCESSOR DECOUPLING
			Size: Document Number: ZAMB0 Rev: 0.1
			Date: Friday, March 07, 2014 Sheet 49 of 50

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2015/07/08

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Compal Electronics, Inc.		
Title: PWR-PIR		
Size	Document Number: ZAMB0	Rev: 0.1
Date: Friday, March 07, 2014	Sheet 50 of 50	